A Segmented Current Steering DAC for Wireless Application

Vivek P. Landge, (M.Tech.)
NYSS College of Engineering and Research, Nagpur. (M.S.)

Abhijit B. Maidamwar (M.Tech.)
NYSS College of Engineering and Research, Nagpur. (M.S.)

ABSTRACT
This paper presents a CMOS Nyquist Rate Current Steering DAC using segmented architecture for wireless application. Segmentation is used to improve the dynamic behavior of the converter but comes at a cost. The proposed DAC adapts 8-4 segmentation architecture to achieve high speed. The DAC is realized in 0.18-µm CMOS process and the power supply used is 1.8V. Cadence Virtuoso Schematic editor is used for drawing the schematic of various circuits and the circuits are simulated using Virtuoso circuit simulator. The DAC has been simulated and found to be working satisfactorily.

General Terms
Digital to Analog Converter, binary weighted DAC, Thermometer coded DAC.

Keywords
DAC, Unit current source, DNL, glitch, clock skew, clock feedthrough.

1. INTRODUCTION
Throughout the years there has been an increase in demand for high speed communications, which has created a great demand on high-performance data converters. Data converters poses so many challenges due to ever increasing need for high bit rates. The conventional view of data converters as numerical conversion blocks does not suffice for wireless applications. From a wireless system's perspective, the bit error rate (BER) requirement determines the signal-to-noise ratio (SNR) requirement for a given modulation and duplexing scheme. Therefore, when we design data converters for a wireless application, frequency- domain measures such as the SNR are of great importance.

The wireless device uses Orthogonal Frequency Division Modulation (OFDM) where data is modulated onto a number of carriers or tones by using for Example Quadrature Amplitude Modulation (QAM) on each tone. The current steering DACs are much faster and have very high power efficiency since almost all power is directed to the output. The basic structure needs no feedback hence the bandwidth is large. Hence current steering DAC using segmented architecture is used in wireless applications.

2. DAC Architecture
In the binary implementation, the digital inputs directly control the switches. The advantage of binary weighted DAC is its simplicity, as no decoding logic is required. However, there are several major drawbacks associated with major bit transitions. At the mid-code transition, the most significant bit current source needs to be matched to the sum of all the other current sources to within 0.5 least significant bit. This is difficult to achieve, because of statistical spread, such matching can never be guaranteed. Therefore this architecture is not guaranteed to be monotonic. The errors caused by the dynamic behavior of the switches (such as charge injection and clock feedthrough) result in glitches in the output signal. This problem is most severe at the mid-code transition.

In the thermometer-code implementation, each unit current source is connected to a switch controlled by the signal coming from the binary to thermometer decoder. When the digital input increases by 1 LSB, one more current source is switched from the negative to the positive side. Hence, monotonicity is guaranteed using this architecture. The matching requirement is much relaxed. At the mid-code a 1 LSB transition causes only one current source to switch as the digital input only increases by one. This greatly reduces the glitch problem. Glitches hardly contribute to nonlinearity in the thermometer coded DAC. One major drawback of the thermometer coded DAC is area and power consumption. To achieve a good DNL specification and glitch energy, the number of bits implemented in the binary weighted part of the DAC has to be small. However for every extra bit implemented in the unity decoded part, the number of control lines needed to select the current sources doubles and the decoding logic complexity increases significantly. A direct consequence is often a reduction in the maximum operating speed. To get the best of both architectures, Digital to Analog Converter is implemented using a segmented architecture.

The input signals are split up so that 4 bits are passed directly to the latches and 8 bits go through the binary-to-thermometer decoder as shown in figure 1. The binary-to-thermometer decoder generates 255 control signals, which are then put in to the latch network. From the latches the 4 binary bits are fed to their respective switch and the 255 control signals go into their switches. The switches are connected to the current sources. The main matrix consists of 255 thermometer current sources and 15 binary current sources. The matrix consists of three types of rows. They are:

1) Rows in which all of the current cells are turned on;
2) Rows in which all of the current cells are turned off; and
3) A certain row in which current cells are turned on depending upon the column decoder signal.

In consideration of these three types of rows, a decoding logic, which is carried out in two steps has been developed as shown in figure 2.

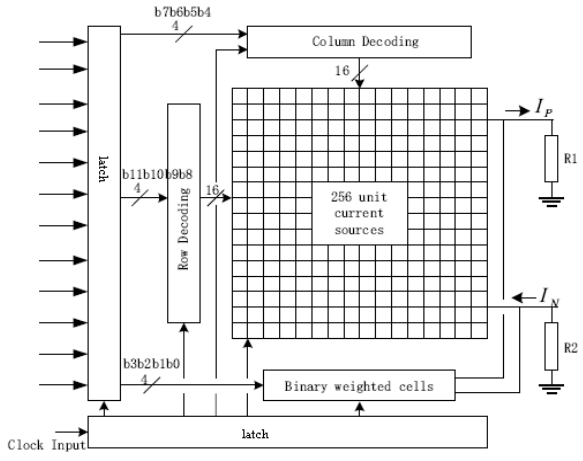

Figure 1: Basic block diagram of the entire DAC system

R_i	R_{i-1}	C_i	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

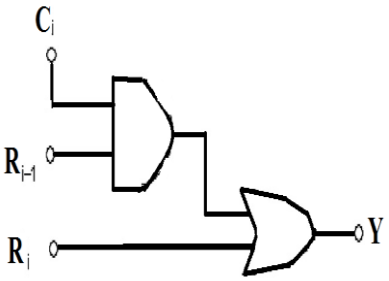

Figure 2: Truth table and decoding logic for each current cell.

3. Unit Current Source

The unit current source is designed to satisfy the random mismatch requirements as shown in figure 3.

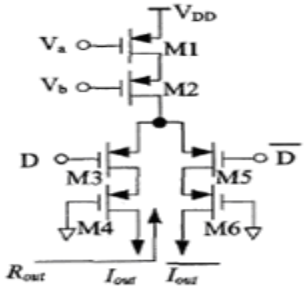

Figure 3: Circuit Diagram of Unit current cell

The glitch is a major problem in unit current cell design. Glitch makes noise larger and affects circuit settling time. Some important issues that have been identified to cause glitch are:
1) Non-synchronization of input signal;
2) Switches in the off-state at the same time;
3) Coupling of the control signals through the C_{GD} of the switches to the output;
4) Output voltage variation of current source;

First, this problem was solved by placing a deglitch circuit in front of the switch. In this way, any delay introduced by the digital decoding logic can be circumvented. Second, this problem was solved by the use of two inverters. These circuits rise the cross point of the control signals of switches. As soon as one of the switching transistors begins to switch off, the complementary switching transistor starts to switch on. Third, this problem was solved by placing a cascade transistor on top of the switch. For a low-to-high transition of the control signal, while the switching transistor is forming a channel, the cascode transistors are off and the signal path from the drain of the switching transistor to the output node is open. The coupling is therefore avoided. For a high-to-low transition, some coupling exists at the beginning. Since the switching transistor cuts off very rapidly, the voltage at the source of the cascode transistor drops, turning it off, and isolating the output node for the remaining of the transition of the control signals. Fourth, this problem was solved by using cascode current source. This method can improve the input resistance of the current source, so the output voltage variation can be suppressed.

4. BINARY TO THERMOMETER DECODER

The logic diagram for binary to thermometer decoder is shown in figure 4.

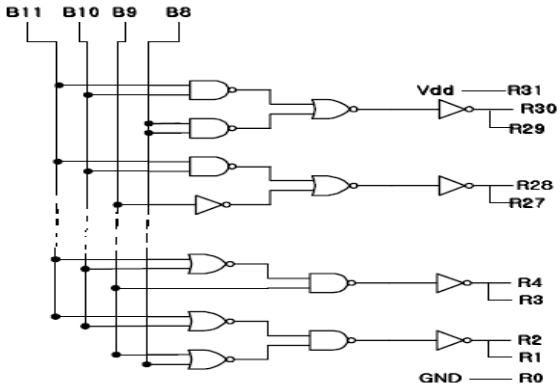

Figure 4.a: Row decoder

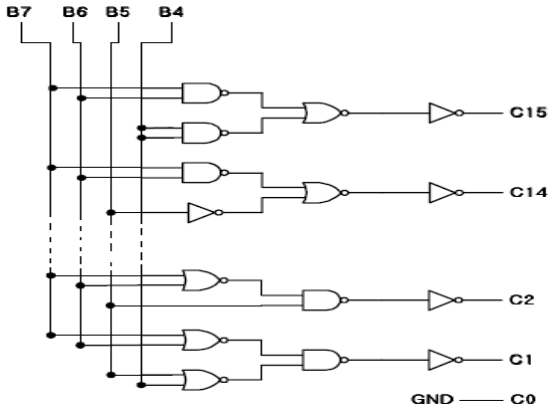

Figure 4.b: Column decoder
Figure 4 : 4-bit Binary to thermometer decoder logic diagram

5. COMPLETE CURRENT BLOCK IN THERMOMETER CODED DAC

The complete current blocked used in the thermometer coded architecture is shown in the figure 5. It shows the switching current source along with the driver. The problems causing a degradation of the dynamic performance of a current steering DAC can be solved by the use of synchronized driver placed immediately in front of the switches. The main function of this driver is the shifting of the crossing point of the switch transistor control signals so that these transistors are never simultaneously in the off-state. Since the driver is clocked and placed immediately in front of the switches, the delay introduced by the digital decoding logic -leading to a timing difference between the control signals of the switches - can be circumvented. Furthermore, the glitch energy error caused by the C_{GD} feed-through is significantly lowered by the use of a reduced voltage swing at the input of the switches.

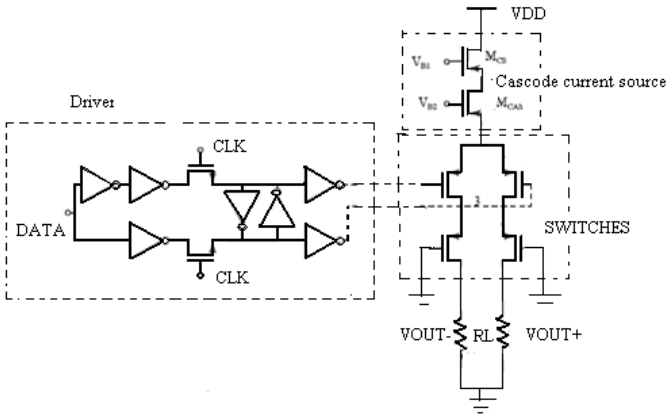

Figure 5: Complete Current Block

6. SCHEMATIC OF COMPLETE BLOCK DIAGRAM

The figure 6 shows the schematic of complete block used. It consist of two blocks binary weighed DAC and thermometer coded DAC. First 8 MSBs are given to thermometer coded DAC and 4 LSBs are given to the binary weighted DAC

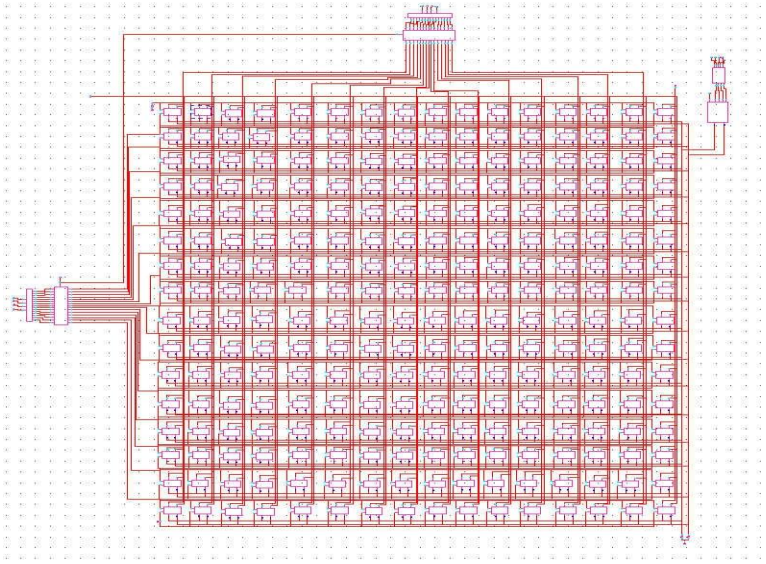

Figure 6: Complete Schematic of Segmented Current Steering DAC Used

7. SCHEMATIC OF SINGLE CURRENT BLOCK

The figure 7 shows the schematic of single current block used in the thermometer coded DAC architecture. The crossing point is obtained so that at no time both blocks are off and reduces the glitch problem.

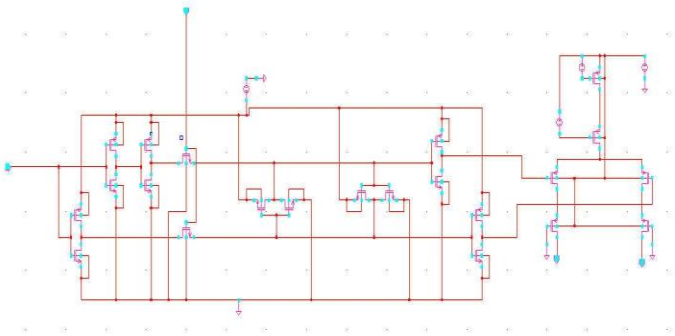

Figure 7: Shows the Schematic of MSB Current Block

8. EXPERIMENTAL RESULTS

8.1 Settling Time Testing:

The figure 8 shows the settling time of the complete DAC found to be 4.89 ns which assures the conversion rate of **200 MSPS**

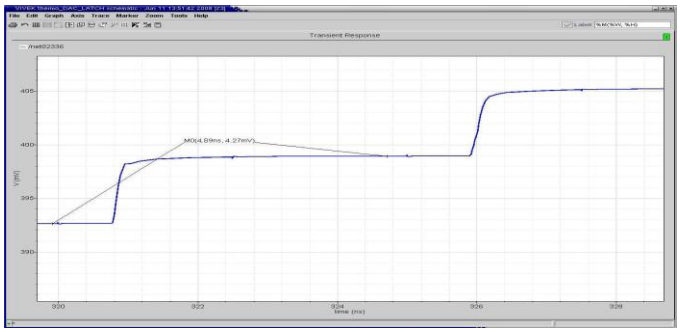

Figure 8: Shows the Settling Time measured as 4.89ns.

8.2 Complete DAC Output Testing

The figure 9 shows the transient response of the complete DAC.

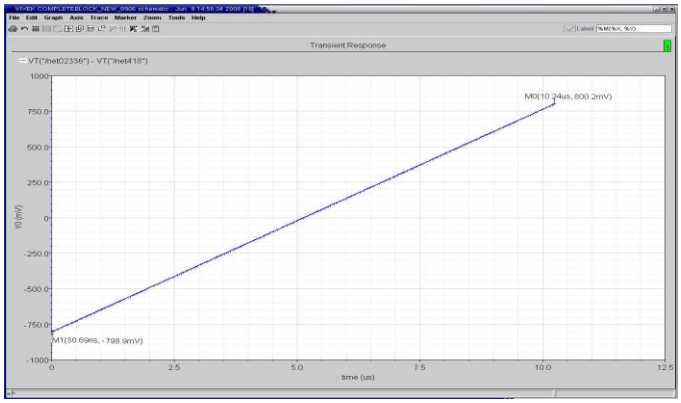

Figure 9: Shows the output of DAC for linear input bits from all Zero's to all One's

9. CONCLUSION

The Current Steering DAC using Segmented Architecture is presented. The DAC is implemented in 0.18um CMOS Technology using Cadence Virtuoso schematic editor and simulator. It has been observed that clock feedthrough and clock skew between MSB and LSB bits are main cause of degradation of performance of DAC.A latch is used to reduce the skew between MSB and LSB bits. The problem of glitch is reduced by proper synchronization of all the bits in the DAC. The area and power consumption of current steering DAC is more and it requires complex routing along the current blocks in the thermometer coded DAC.

10. REFERENCES

[1] M. Gustavsson, J. Wikner, and N. Tan, CMOS Data Converter for Communication. Kluwer Academic Publishers, 2002.

[2] J. Rabaey, Digital Integrated Circuits – A Design Perspective, Prentice Hall, Upper Saddle River, NJ, USA, 1996, ISBN 0-13-394271-6..

[3] M.J.M Pelgrom, A.C.J. Duinmaijer, and A.P.G. Welbers, "Matching Properties of MOS Transistors," IEEE J. of Solid-State Circuits, vol. 24, no. 5, pp. 1433-9, Oct. 1989.

[4] Douglas Mercer, "A Study Of Error Sources In Current Steering Digital-to-Analog Converters", IEEE 2004 Custom Integrated Circuits Conference.

[5] J. Wikner and N. Tan, "A CMOS Digital-to-Analog Converter Chipset for Telecommunication,"IEEE Magazine on Circuits and Devices, Vol. 13, No. 5, pp. 11-16, Sep. 1997.

[6] K.O. Andersson and J.J. Wikner, "Modeling of the Influence of Graded Element Matching Errors in CMOS Current-Steering DACs," in Proc. of the 17th NorChip Conf., NORCHIP'99, Oslo,Norway, Nov. 8-9, 1999.

[7] Ming-Chin Chen, Chia-Chun Liu, and Ching-Cheng Tien, "A 10-bit 160-MSPS 2.5-V Segmented Current Steering CMOS DAC for WLAN Applications ", 2004 IEEE Asia-Pacific Conference on Advanced System Integrated Circuits(AP-ASIC2004)/ Aug. 4-5, 2004.

[8] Nicola Ghittori, Andrea Vigna, Piero Malcovati, Stefano D'Amico, and Andrea Baschirotto, "1.2-V Low-Power Multi-Mode DAC+Filter Blocks for Reconfigurable (WLAN/UMTS, WLAN/Bluetooth) Transmitters", IEEE Journal Of Solid-State Circuits, Vol. 41, No. 9, September 2006.

[9] Gaurav Raja and Basabi Bhaumik**, "**16-bit Segmented Type Current Steering DAC for Video Applications**",** Proceedings of the 19th International Conference on VLSI Design (VLSID'06).

[10] Matthew Gast, 802.11 Wireless Networks, The Definitive Guide- Second Edition, O'reilly Publishing Company. ISBN 0-596-19952-3

[11] Jim Geier, Wireless LANs, Second Edition, Sams Publisher, ISBN 0-072- 32058-4

[12] Ken Martin, "Analog Integrated Circuit Design", John Wiley and Son's Inc.

[13] Ramji Prasad and Richard van Nee, "OFDM for Wireless Multimedia Communications", Artech House universal personal communication Series