Design of Low Power Sram using Adiabatic Change of Wordline Voltage

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ABSTRACT

The requirements of low power integrated circuits are very important in all electronic portable equipment's. Normally SRAM consume more power during read and write operations because of more power consumptions speed of the circuit will be reduced finally the performance will be degraded. To reduce power consumption and increase RNM (Read Noise Margin) the adiabatic change of word line voltage is used in single bit line SRAM and also sense amplifier flip flop and pre-charge circuit is used. During read operation pre-charge circuit is connected with selective bit lines to minimize the overall RAM power consumption and sense amplifier flip-flop is used to increase the speed of the operation. Using of adiabatic circuit in single bit line SRAM, the power consumption is reduced from 80% to 50%.

Index Terms

SRAM, RNM, Sense amplifier flip flop, adiabatic logic.

1. INTRODUTION

The growing demand of portable battery operated systems has made energy efficient processors a necessity. For applications like wearable computing energy efficiency takes top most priority. These embedded systems need repeated charging of their batteries. The problem is more severe in the wireless sensor networks which are deployed for monitoring the environmental parameters. These systems may not have access for recharging of batteries. We know that on chip memories determine the power dissipation of SoC chips. Hence it is very important to have low power and energy efficient and stable SRAM which is mainly used for on chip memories.

There are various approaches that are adopted to reduce power dissipation, like design of circuits with power supply voltage scaling, power gating method. Lower power supply voltage reduces the dynamic power in quadratic fashion and leakage power in exponential way. But power supply voltage scaling results in reduced noise margin. Many SRAM arrays are based on minimizing the active capacitance and reducing the swing voltage. The power loss during reading is more than the power loss during writing in conventional SRAM since there is full swing of voltage in bit lines whereas the bit line voltage swing is very less during reading. The power dissipated in bit lines represents about 60% of the total dynamic power consumption during a read operation. The power consumption by bit lines during writing is proportional to the bit line capacitance, square of the bit line voltage and the frequency of writing.

Power loss is reduced by limiting voltage differences across conducting devices. This is accomplished through the use of time-varying voltage waveforms. This is also called Adiabatic charging technique. The SRAM working purely on adiabatic charging principles need multiple phase power clocks. To increase the RNM by reducing the power consumption in single bit-line SRAM using adiabatic change of word-line.

It is necessary that in addition to saving power in SRAMs care should be taken to see the performance parameters are not much affected. In this Project has been made to reducing the power stored in the bit lines and reused it by adiabatic logic principles. This has been made possible by using a very simple, small and efficient adiabatic driver for charging and discharging the bit lines. The adiabatic driver is driven by a D.C power clock which enables the charging and discharging of the bit lines based on the signal input. Hence the loss of power to the ground during '1'to'0' transition in SRAM is reduced to a great extent. No separate pre-charging circuit is used before or after reading. No synchronization circuit is needed as only bit lines are concerned. Low power sense amplifier is utilized to sense the data. The design of the conventional SRAM can be retained except the write driver and the pre-charge circuit. With this adiabatic logic circuit working in conjunction with conventional SRAM cell other performance characteristics like power, Noise Margin ,read and write delay have been found by simulation in addition to power saving is achieved under varied conditions of memory operations. The effect of device parameters of the circuit on power, RNM and delay of the SRAM cell has been investigated.

2. PROBLEM STATEMENT

Power consumption and timing delays are the two important design parameters in high speed VLSI systems. In many power consumption components digital, the memory system that consists of pre-charge circuit and sense amplifier flip-flops.

3. TWO BIT-LINE SRAM DESIGN

Static random-access memory is a type of semiconductor memory that uses bi-stable latching circuitry to store each bit. The term static differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. SRAM exhibits data remanence, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered.

A typical SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors (M1, M2, M3, M4) that form two cross-coupled inverters. Two additional access transistors serve to control the access to a storage cell during read and write operations. The structure of a 6 transistor SRAM cell with dual bit line, storing one bit of information, can be seen in Figure1.1 the core of the cell is formed by two CMOS inverters, where the output potential of

each inverter Q is fed as input into the other Qbar. This feedback loop stabilizes the inverters to their respective state. The access transistors and the word and bit lines, WL and BL, are used to read and write from or to the cell. In standby mode the word line is low, turning the access transistors off. In this state the inverters are in complementary state. When the p-channel MOSFET of the left inverter is turned on, the potential Qbar is high and the p-channel MOSFET of inverter two is turned off, Q is low. To write information the data is imposed on the bit line and the inverse data on the inverse bit line, BLbar. Then the access transistors are turned on by setting the word line to high. As the driver of the bit lines is much stronger it can assert the inverter transistors. As soon as the information is stored in the inverters, the access transistors can be turned off and the information in the inverter is preserved. For reading the word line is turned on to activate the access transistors while the information is sensed at the bit lines.
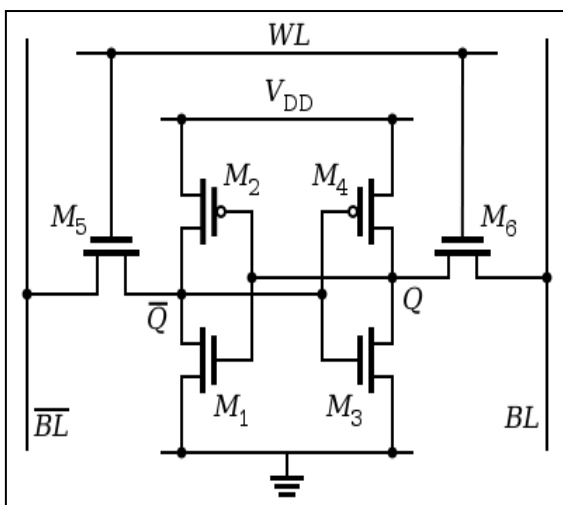

Fig.1. Design of SRAM with Dual Bit Line

4. DESIGN OF SINGLE BIT-LINE SRAM

Single bit-line SRAM is same as the two bit-line SRAM but single bit-line SRAM having several advantages based on their design, reduction in cell area and power consumption and reduction in read delay, write delay. The cell area decreases by one transistor and one bit line. The power consumption from charging the bit line decreases by approximately a factor of 2 because only one bit line is charged during a read operation instead of two, and the bit line is charged during a write operation about half of the time (assume equal probability of writing 0 and 1) instead of every time when a write operation is required.
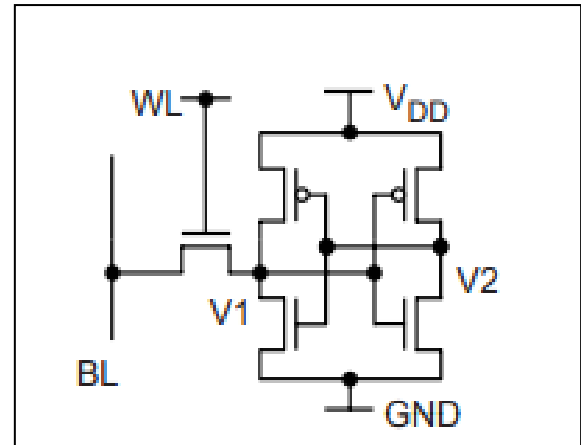

Fig.2. Design of Single Bit-Line SRAM

A single-BL SRAM Figure4.3 uses only one BL for reading. When $V1 = 1$ and $V 2 = 0$, V2 is not connected to the pre charged BL; so it remains at a low level. Therefore, a single-BL SRAM has a larger SNM than one with two BLs. To examine the effect of adiabatically charging, we assume that the capacitance of a BL is small and that the voltage of a BL decreases from the pre charge voltage to 0 because the initial conditions are $V1 = 0$ and $V2 = 1$. In a conventional SRAM, WL charges abruptly, resulting in a large change in V1 because a large current flows from the BL to the V1 node. This destabilizes the FF. In contrast, if the WL charges adiabatically, V1 remains close to the GND level, Thus, the FF is stable. Assumed that the voltage of the WL gradually changed from GND to VDD, and that the voltage of the BL connected to the low-voltage node of the FF gradually changed from the pre charge voltage to GND Fig.2.Then, we calculated the DNM from the initial to the final state. We calculated input–output curves for the two inverters in the FF: for one inverter, the input voltage is V1 and the output voltage is V2; and for the other, the values are reversed.

5. DESIGN OF SINGLE BIT-LINE SRAM USING ADIABATIC LOGIC

In this circuit one can ensure that both the bit lines are charged to the same voltages before reading. The various steps involved in writing, reading and hold operations in the new circuit. In both the conventional SRAM and the proposed adiabatic SRAM, the data which has to be written is first obtained with its complement using two inverting buffers as shown in Fig.3.
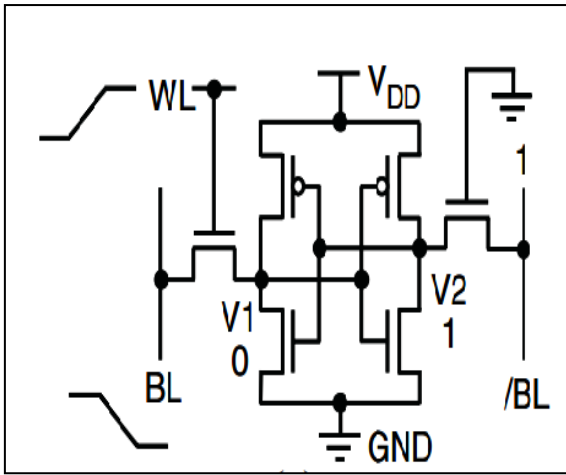
Fig.3. Design of Single Bit-Line SRAM using Adiabatic Logic

A low power RAM device including a bit line pre charge circuit which selectively pre charges only those bit lines which will be read in an effort to minimize pre charge and overall RAM power consumption. The preferred RAM pre charge circuit uses a pre charge device in the sense amplifier as the primary bit line pre charge device to selectively connect and pre charge the selected bit line through a column MUX. The preferred RAM pre charge also includes secondary bit line pre charge devices for each bit line to enable trickle charging thereof to prevent hazardous RAM data corruption. Since RAM corruption occurs only after several clock cycles, the secondary pre charge devices comprise small transistors having only 1/20 the size of normal pre charge device to conserve pre charge power requirements.
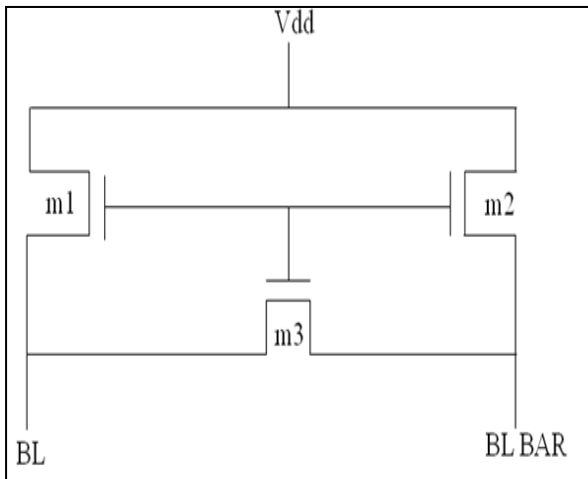

Fig.4. Pre-charge circuit

The RAM device includes a carefully controlled timing sequence of pre charge signal, column-select signals, and word-line signals, to selective pre charge the selected bit line and to remove the hazardous power consuming DC current path to further reduce power consumption.

Sense amplifier is a regenerative structure like a latch which speeds up the generation of the output. It is basically a simple regenerative differential amplifier as shown in the Fig.5. It compares the difference between the voltage levels of bit and bit bar lines. The sense amplifier changes its output even with small difference between the bit lines. The figure also shows

how the sense amplifiers are coupled to the bit lines through two switches which are enabled only during a short period of read time by the clock signal. Then the data is latched.
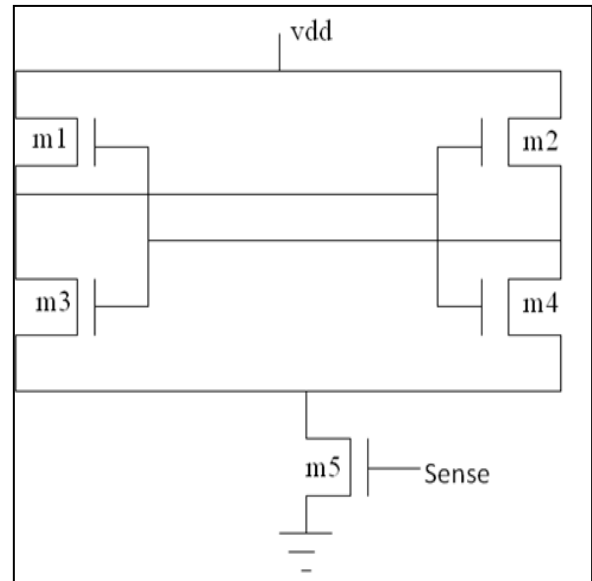

Fig.5.Sense Amplifier Flip-Flop

6. SIMULATION RESULTS

Schematic design and simulation results of two bit-line SRAM, single bit-line SRAM and single bit-line SRAM using adiabatic logic designs are shown below. All the SRAMs were designed using Tanner 15.0v's, Generic 250nm technology, at an operating temperature of 27ºC and a supply voltage of 2.5 V. The power consumption of the SRAM is measured using print power command line in the T-Spice net list. Calculation for RNM(Read Noise Margin) , energy and bandwidth for the single bit-line SRAM using adiabatic logic is given below. And the results were analyzed for higher and lower switching activity.
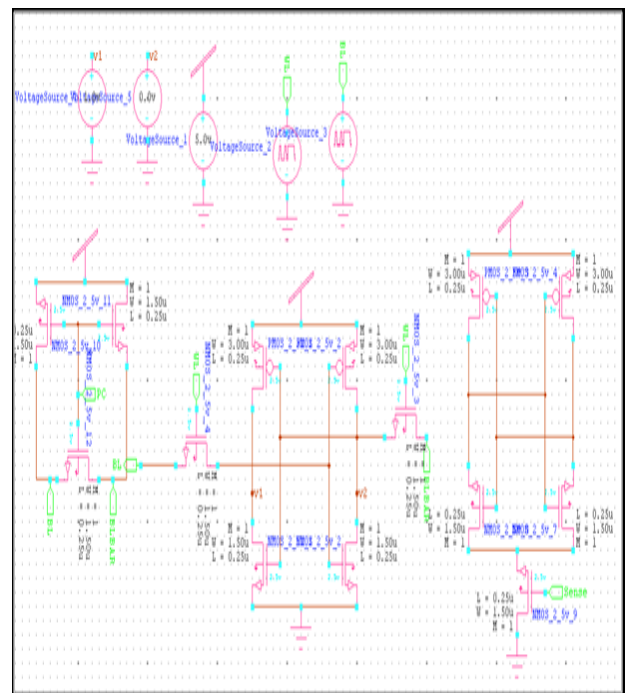
Fig.6. Schematic Design of Two Bit-Line SRAM
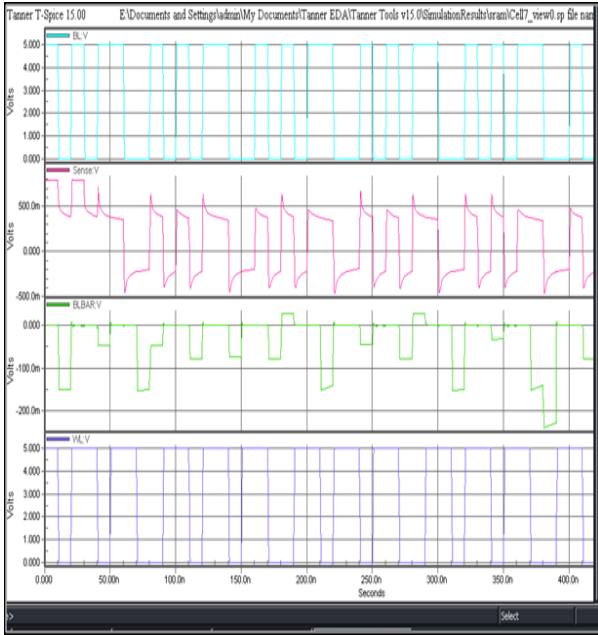
Fig.7. Simulation output of Two Bit-Line SRAM Design

Two Bit-Line SRAM power consumption is shown in below Fig.8. two bit-line SRAM power consumption is calculated by using print Voltage Source power command line in T-Spice of Tanner 15.0v tool.
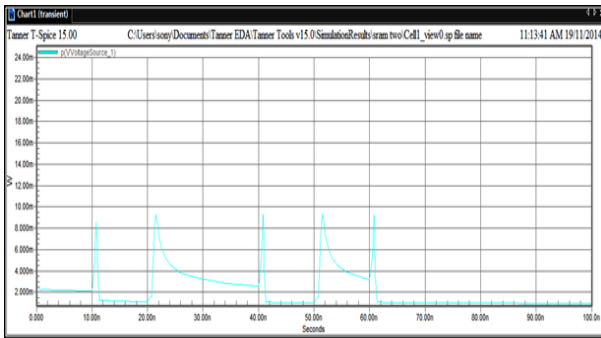
Fig.8. Power Results
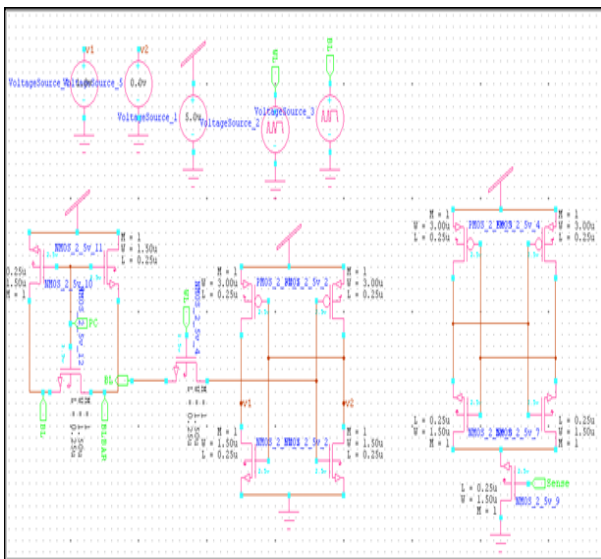
Fig.9. Schematic Design of Single Bit-Line SRAM

When V1=0, V2=1 then V2 is not connected to the pre charged BL so it remains low level. Therefore single BL SRAM has a larger SNM than two BL SRAM. here Sense is an output line for both read and write operation.
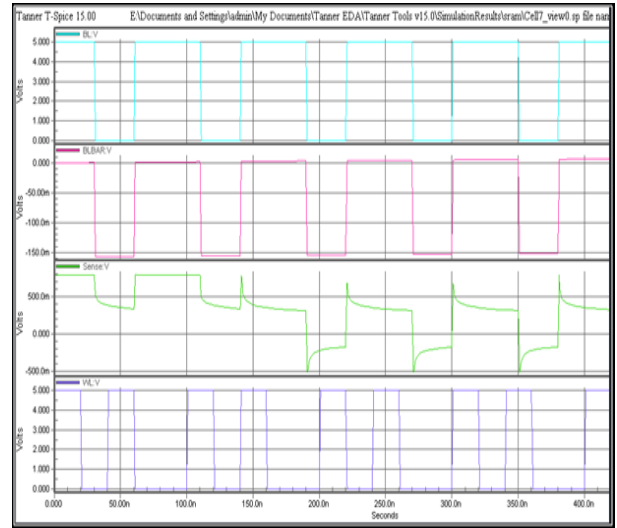
Fig.10. Simulation output of Single Bit-Line SRAM Read Operation Design
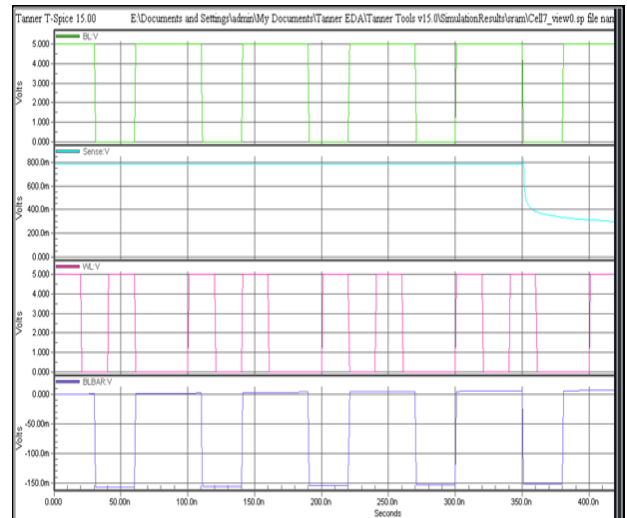
Fig.11. Simulation output of Single Bit-Line SRAM Write Operation Design

Fig.12. Power Results

Fig.13. Schematic Design of Single Bit-Line SRAM Using Adiabatic Circuit Design

Based on whether adiabatic charging is applied to only power supply line or ground line or bit lines and word lines, there are many types of adiabatic SRAMs.

Fig.14. Simulation output of Single Bit-Line SRAM Using Adiabatic Circuit Read Operation Design

Fig.15. Simulation output of Single Bit-Line SRAM Using Adiabatic Circuit Read Operation Design

Single Bit-Line SRAM using adiabatic logic read and write operation power is calculated by using print power command line in T-Spice and it consumes less power compared to an normal single Bit-line SRAM and two Bit-line SRAM.

Fig.16. Power Results
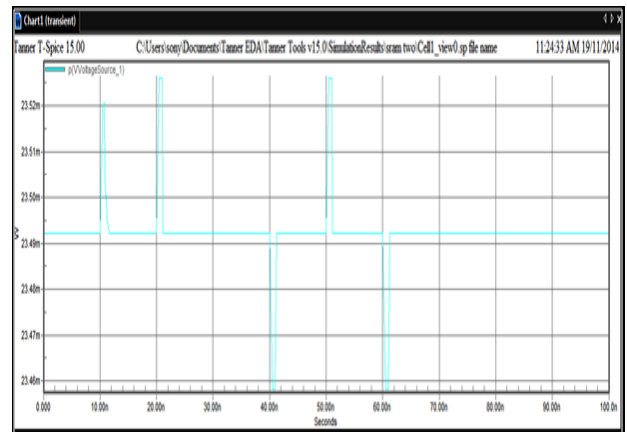
FORMULA USED
Read Noise Margin Calculation

$$\sigma V_{TH} \quad \alpha \quad [WL]^{-1/2} \ V_{TH}$$

$$\sigma_i^2 \qquad = \sigma V_{THo} \ (\sqrt{} \ Wmin \ . \ Lmin/WL)$$

Where,

$\sigma V_{THo} = 0.7 \ V, \ Wmin = 2 \ Lmin = 100 \ , W = 1.5u \ L = 0.25u$

$$\sigma_i^2 \qquad = \quad 0.375$$

$$NM \qquad = \quad \sigma^2 SNM$$

$SNM \qquad = \quad Input \ Voltage – Output \ Voltage \qquad = 5 – 5*10^{-3}$

$$= \quad 4.995V$$

$$\sigma^2_{SNM} \qquad = \quad \Sigma^6_{i=1} \ \sigma_i^2 \ (\partial SNM \ / \ \partial V_{thi})^2$$

$$= \quad \{((\partial SNM \ / \ \partial V_{th1})^2) + (\partial SNM \ / \ \partial V_{th2})^2\} \ \sigma^2_{drv} + \{((\partial SNM \ / \ \partial V_{th3})^2) + (\partial SNM \ / \ \partial V_{th4})^2\} \ \sigma^2_{load} + \{((\partial SNM \ / \ \partial V_{th5})^2) + (\partial SNM \ / \ \partial V_{th6})^2\} \ \sigma^2_{access}$$

$$= \{((0.095 + 0.127) * 0.06)\} + \{((0.063 + 0.190) * 0.06)\}\{((0.042 + 0.047) * 0.06)\}$$

$$= \quad 33mV$$

Bandwidth Calculation

$BW \qquad = \quad F_H \text{ - } F_L$
$\qquad\qquad = \quad 80 – 40 \ (MHZ)$

$$= \quad 40 \ MHZ$$

Where,

BW – Band Width

F_H – High Frequency

F_L – Low Frequency

Energy Calculation

$E \qquad = \quad E_{Classic} + E_{Adiabatic}$

Where,

E   – Energy

E $_{Classic}$ – Classic Energy

E $_{Adiabatic}$ – Adiabatic Energy

$E = CV^2 + 2\,(RC/T)\,CV^2$

C=1pF, V=5V, R=10KΩ, T=100nS

$E = 2.5 * 10^{-11} + 0.133$

   = 5pJ

Para-meters	Two Bit-Line SRAM		Single Bit-Line SRAM		Single Bit-Line SRAM using Adiabatic Logic	
	Read	Write	Read	Write	Read	Write
Power (W)	2.142 (m)	2.142 (m)	0.234 (m)	0.234 (m)	0.194 (u)	0.189 (u)
Delay (nS)	1.70	1.70	0.68	0.68	0.45	0.45

Fig.17.Tabulation for power and delay

RNM (mV)	Energy (pJ)	Band Width (HZ)
33	5	40

Fig.18.Tabulation for RNM, Energy and Bandwidth

7. CONCLUSION

Power consumption has become a very important issue for VLSI designers. To improve the Read Noise Margin and reducing the power consumption, 5T SRAM cell has been designed and realized using adiabatic approach. The 5T SRAM is realized by using asymmetrical design for SRAM cell with single ended reading approach. Since no pre-charge line is used for before or after reading. This asymmetrical design improves the noise margin of the SRAM. The single ended sense amplifier consists of two buffers of sizes in increasing order. Adiabatic driver recovers energy during '1'to'0' write operation. Single Bit-Line SRAM, consumes about 50% of total power and 80% power during write cycle can be saved by the adiabatic circuit.

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