A Pursuit of Dynamic Address Alternator for WIMAX Deinterleaver

Yogeesh T.R.
PG Scholar,
VLSI and Embedded Systems
SJCE, Mysuru.

Shreekanth T.
Assistant Professor,
Dept of Electronics and Communication
SJCE, Mysuru

ABSTRACT
In the modern communication system, the variety of technology leads to the developmental concepts and for that wireless technology also plays a prominent role in the field of modern communication. WiMAX has got its own limitation. The key difficulty is Deinterleaver design and it needs ample hardware if all the modern schemes and code rates have to be designed on field programmable gate array (FPGA). Floor function is one such design with a great degree impotence of hardware. This paper is an attempt to have a variable newer technology and to regulate the impotence of the hardware. Mathematical model has been done in order to remove hardware impotence and by introducing embedded multiplier in FPGA interconnection delay has been reduced .The internal multiplier of FPGA along with 16QAM and 64 QAM modulations have made this connectivity novel and efficient.

General term
Digital Circuits, Wireless Systems.

Keywords
WiMAX (Worldwide interoperatability for microwave access), Deinterleaving.

1. INTRODUCTION
In the current trend broadband remote access is one of the aids to the correspondence territory. This is additionally difficult to customary wired last mile access innovation [1]. WiMAX is a propelled, very much created standard for portable, broadband remote access .It has got a key part in minimizing the burst blunder impact [2]. WiMAX contains transreceiver and it has an unmistakable part to set up a well standard innovation.

WiMAX is one of the most sizzling remote broadband advances around today. WiMAX frameworks are relied upon to convey broadband access to private and venture clients in a practical way. All the more entirely, WiMAX is an industry exchange association framed by driving correspondences, segment and gear organizations to advance and guarantee similarity and interoperability of remote broadband access hardware that complies with the IEEE 802.16 and ETSI HIPERMAN standard. WiMAX could work like wifi however at higher speeds over more noteworthy separation and more prominent number of clients.

It gives improvement in sight and sound information administrations and Quality of Service (QoS). It underpins synchronous voice, information, and sight and sound administrations to a huge gathering of endorsers. WiMAX additionally offers a rich arrangement of elements with parcel of adaptability as far as organization alternatives and potential administration offerings. The WiMAX physical layer is taking into account Orthogonal Frequency Division Multiplexing which offers a decent resistance for multipath and permits WiMAX to work in Non Line of Sight (NLOS) conditions.

Comparing with conventional study and LUT based techniques. The LUT technique confirms the superiority of the design proposed. By the virtue of 2D translation it has become user friendly with a mathematical representation and subsequent algorithm that too particularly for 64 QAM (Quadrature Amplitude Modulation) and 16 QAM [6].The proposed algorithm results a low complexity architecture compared to a previous techniques.

This novel proposed hardware is for more better than any other conventional type a detailed view is here with presented the authors adopted with detailed look and shared the optimization by way of comparing common hardware [6] and modules for Quadrature Phase Shift Keying (QPSK) ,16 QAM and 64 QAM. Very long made architecture and it is implemented of the Xilinx Spartan 3 FPGA by using Xilinx Isim software simulation is checked in order to know the functionality of the hardware and proposed algorithm on checking FPGA implementation results have been compared with the recent similar works.

In brief the performance of WiMAX is a well improved technology and it provides a novelistic, high speed access and on reducing interconnection delay. It efficiently works with a lesser power consumption compared to a configurable logic block based multiplier. The work done by us will give light in the technology of getting the betterment for maximum operating frequency.

2. SYSTEM OVERVIEW
The transfer of information bearing signal from source to destination via communication channel may be by guided or unguided medium is the main objective of communication system. In Figure 1, it is shown that the mandatory blocks of WiMAX transceiver system.

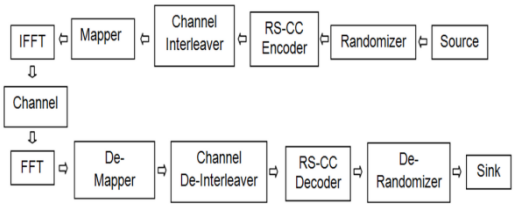


Figure 1: WiMAX Transreceiver block diagram.

The data which enters into the randomizer is the MAC payload data units (PDU's) which randomizes the data when the randomized data enters the encoder .it is coded by using the reed Solomon and convolution encoder. The data is mapped into QAM symbol after it is interleaved by the interleaver. OFDM modulation consists of OFDM frame, 256 IFFT into which the mapped data enter. Then the mapped data is transmitted over the channel. The order to get back the original data, it undergoes the reverse process in the receiver. In this work our focus is on designing algorithm for channel Interleaver/Deinterleaver. The block Interleaver/Deinterleaver

structure, which is used as a channel Interleaver/Deinterleaver in the WiMAX system, is described in Figure 2.

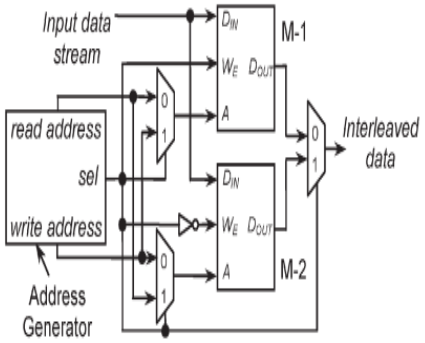


Figure 2: Structure of interleaver/deinterleaver

The two-dimensional block Interleaver /Deinterleaver structure used in the WiMAX system is as shown in above diagram. Here this structure consists of two memory blocks namely M-1, M-2 and an address generator block. It also consists of two multiplexer associated with each memory block and these multiplexers are used to select the lines depending upon read and write operation. The not gate symbol used depicts the inversion of operation that shifts from read to the write. Note that the select line is given and when it is 1, write enabled signal will be active of M-1. During this period, the input data stream is written. And when the select line is 0, the read enabled signal will be active hence during this process; input data stream is read from M-2.

After the memory blocks are written/read up to the desired location as specified by the Interleaver depth, the status of select signal is changed to swap the read/write operation. For all the permissible code rates and the different modulation schemes used in WiMAX system, the permitted Interleaver/Deinterleaver depth according to IEEE 802.16e [10] standard, the Table 1 shows the Interleaver/Deinterleaver depths.

Table 1: Depths of Interleaver/Deinterleaver

Modulation Scheme	QPSK (s=1)		16-QAM (s=2)		64-QAM (s=3)		
Code Rate	½	¾	½	¾	½	⅔	¾
Interleaver Depth, N_{cbps} in bits	96	144	192	288	288	384	432
	192	288	384	576	576	-	-
	288	432	576	-	-	-	-
	384	576	-	-	-	-	-
	480	-	-	-	-	-	-
	576	-	-	-	-	-	-

The formula that are used in interleaving process is given as below

$$mk = \left(\frac{Ncbps}{d}\right) * (k\%d) + \left\lfloor\frac{k}{d}\right\rfloor \quad (1)$$

$$jk = s * \left\lfloor\frac{mk}{s}\right\rfloor + \left(mk + Ncbps - \left\lfloor\frac{d.mk}{Ncbps}\right\rfloor\right)\%s \quad (2)$$

Here the number of columns is represented by d (= 16/12) where mk and jk are the output of the first and second steps respectively, and 'k' varies from 0 to Ncbps-1. 's' is a parameter defined as s=Ncpc/2. Where Ncpc is the number of coded bits per subcarrier that is 2, 4, and 6 for QPSK, 16-QAM, 64-QAM respectively [9]

Similarly the formula that can be used for deinterleaving process of WiMAX system is given by,

$$mj = s * \left\lfloor\frac{j}{s}\right\rfloor + \left(j + \left\lfloor\frac{d.j}{Ncbps}\right\rfloor\right)\%s \quad (3)$$

$$kj = d.mj - (Ncbps - 1) * \left\lfloor\frac{d.mj}{Ncbps}\right\rfloor \quad (4)$$

The deinterleaver which performs the inverse operation is also defined by two permutations as shown above. Let mj and kj defines the first and second level of permutation for deinterleaver. Where 'j' is the index of the received bits within a block of Ncbps bits.

3. PROPOSED ALGORITHMS

The proposed algorithm for address generator for WiMAX deinterleaver is already been described in above equations. But the problem with this is direct implementation of floor and ceil function is not feasible.

Since there are three different modulation schemes used, we obtain algorithm for each individual modulation scheme as shown below, for generation of address in WiMAX in our proposed work instead of using floor function a two step permutation process is used. By using floor function large amount of resources are need to implement the hardware. By this the circuit will be inefficient. So the two step process is combined to one step in order to make circuit efficient and hence the correlation between input and output is obtained. For this, one dimensional equation is realized into joint two dimensional expressions.

Keeping in mind the end goal to actualize equipment productively, it is not important to change both arrangements of comparisons to 2-D space and execute independently. Since both arrangements of mathematical statements are reverse of one another [11]. So to execute equipment proficiently, one and only arrangement of mathematical statements must be changed and the same can be utilized for other by swapping the request of read and compose of information into memory [6].

The transformation steps for QPSK, 16-QAM, and 64-QAM is shown as below,

The first permutation for index 'n' is given by

$$mn = s * \left\lfloor\frac{n}{s}\right\rfloor + \left(n + \left\lfloor d.\frac{n}{Ncbps}\right\rfloor\right)\%s \quad (5)$$

Similarly the second permutation of index 'n' is given by,

$$kn = d * mn - \left((Ncbps - 1) * \left\lfloor d.\frac{mn}{Ncbps}\right\rfloor\right) \quad (6)$$

These are the formulas used as general of 'n' index bits.

3.1 Algorithm used for QPSK

We know that for QPSK, the parameter s=1

Defining 'N=Ncbps, simplifies (6) to,

$$kn = d * n - \left((N - 1) * \left\lfloor\frac{d*n}{N}\right\rfloor\right) \quad (7)$$

$$kn = d * \left(n - \frac{N}{d} * \left\lfloor\frac{d*n}{N}\right\rfloor\right) + \left\lfloor\frac{d*n}{N}\right\rfloor \quad (8)$$

$$kn = d * \beta n + \gamma n \quad (9)$$

Where beta and gamma n are defined as,

$$\beta n = d * n - \frac{N}{d} + \left\lfloor \frac{d*n}{N} \right\rfloor \quad (10)$$

$$\gamma n = \left\lfloor \frac{d*n}{N} \right\rfloor = \left\lfloor \frac{n}{N/d} \right\rfloor \quad (11)$$

By analyzing behaviour of different terms and verifying for all possible block sixe, re-constructing of equations are done in order to eliminate the floor function.

For example in case of BPSK with two sub channels, d=16 and N=32 is taken and behaviour of beta n is analyzed against the index 'n',

$$\beta n = n - 2 * \left\lfloor \frac{n}{2} \right\rfloor \quad (12)$$

$n = 0\ ,\ \beta n = 0,\ \beta n = (0\%2)$

$n = n\ ,\ \beta n = 1,\ \beta n = (n\%2)$

After checking for all cases of BPSK and QPSK, (i.e. sub channels 1, 2, 4, 8, 16), beta n can be generalized as,

$$\beta n = \left(n\% \frac{N}{d}\right) \quad (13)$$

Thus for QPSK, equation (6) can be written as,

$$kn = d * \left(n\% \frac{N}{d}\right) + \left\lfloor \frac{d*n}{N} \right\rfloor \quad (14)$$

Introducing a two dimensional array, for which 'j' increments for 'i' expires. The ranges for 'j' and 'I' can be selected as,

$\mathrm{i} = 0,1,\ldots \left(\frac{\mathrm{N}}{\mathrm{d}} - 1\right)$ which satisfies against 'n' if $\mathrm{i} = \left(\mathrm{n}\% \frac{\mathrm{N}}{\mathrm{d}}\right)$ (15)

$\mathrm{j} = 0,1,\ldots (\mathrm{d} - 1)$ with behaviour against 'n' if $\mathrm{j} = \left(\frac{\mathrm{n}}{\mathrm{N/d}}\right)$ (16)

The deinterleaver can be realized as a 2-D row-column matrix with size j*i, where the total number of rows id 'd' defined by 'j' and the total number of column is N/d defined by 'i'

Thus equation 6.6 can be written as,

$$kn = ki, j = d * i + j \quad (17)$$

3.2 Algorithm used for 16-QAM

For 16-QAM, the parameter is 2 Therefore equations 5 and 6 can be written as,

$$mn = 2 * \left\lfloor \frac{n}{2} \right\rfloor + \left(n + \left\lfloor d.\frac{n}{Ncbps} \right\rfloor\right)\%2 \quad (18)$$

The second permutation for index 'n' is given by,

$$kn = d * \left(mn - \frac{N}{d} * \left\lfloor \frac{d*mn}{N} \right\rfloor\right) + \left\lfloor \frac{d*mn}{N} \right\rfloor \quad (19)$$

The value of beta n and gamma n can be defined as,

$$\beta n = mn - \frac{N}{d} + \left\lfloor \frac{d*mn}{N} \right\rfloor \quad (20)$$

$$\gamma n = \left\lfloor \frac{d*mn}{N} \right\rfloor \quad (21)$$

Therefore,

$$kn = d * \beta n + \gamma n \quad (22)$$

After verifying for all the range of WiMAX, the parameter gamma n can be written as,

$$\gamma n = \left\lfloor \frac{d*mn}{N} \right\rfloor = \left\lfloor \frac{d*n}{N} \right\rfloor = \left\lfloor \frac{n}{N/d} \right\rfloor \quad (23)$$

Using definitions in equation 5 and 12, beta n value can be written as,

$$\beta n = 2 * \left\lfloor \frac{n}{2} \right\rfloor + \left(\left(n + \left\lfloor d.\frac{n}{Ncbps} \right\rfloor\right)\%2\right) - \frac{N}{d} * \left\lfloor \frac{d*n}{N} \right\rfloor \quad (24)$$

By analyzing behaviour of different terms and verifying for the entire possible block size, re-structuring of equations are done in order to eliminate the floor function.

3.3 Algorithm used for QAM-64

For QAM-64, the parameter used is s=3. Therefore equation 5 can be written as,

$$mn = 3 * \left\lfloor \frac{n}{3} \right\rfloor + \left(n + \left\lfloor d.\frac{n}{N} \right\rfloor\right)\%3 \quad (25)$$

Now defining the two terms as in beta n and gamma n, as given in equation 5 and 12, beta n can be defined as,

$$\beta n = 3 * \left\lfloor \frac{n}{3} \right\rfloor + \left(\left(n + \left\lfloor d.\frac{n}{Ncbps} \right\rfloor\right)\%3\right) - \frac{N}{d} * \left\lfloor \frac{d*n}{N} \right\rfloor \quad (26)$$

Re-structuring of the equations is done in order to eliminate the effect of floor function, as done in QAM-16. Therefore,

$$\beta n = r\ i,j = \left[\left(i - j'\right) + \frac{j'\left(j'-1\right)}{2}\right] * i +$$

$$\{[j' - \left(j' - 1\right)\{(i-2)\left[\left(1 - i'\right) + \frac{i'\left(i'-1\right)}{2}\right] + (i-1)[i' - \frac{i'\left(i'-1\right)}{2}]\}\}$$

$$+\{\frac{j'\left(j'-1\right)}{2}\{\ [(i+2)\left[i' - i'^{(i-1)}\right] + (i-1)\left[\left(1 - i'\right) + i'i'-1\}\right. \quad (27)$$

Where i and j are column and row count respectively.

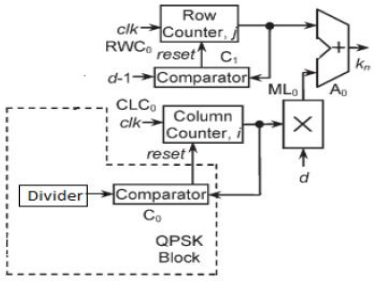
$\mathrm{i} = 0,1,\ldots \left(\frac{\mathrm{N}}{\mathrm{d}} - 1\right)$ which satisfies against 'n' if $\mathrm{i} = \left(\mathrm{n}\% \frac{\mathrm{N}}{\mathrm{d}}\right)$ (28)

$\mathrm{j} = 0,1,\ldots (\mathrm{d} - 1)$ with behaviour against 'n' if $\mathrm{j} = \left(\frac{\mathrm{n}}{\mathrm{N/d}}\right)$ (29)

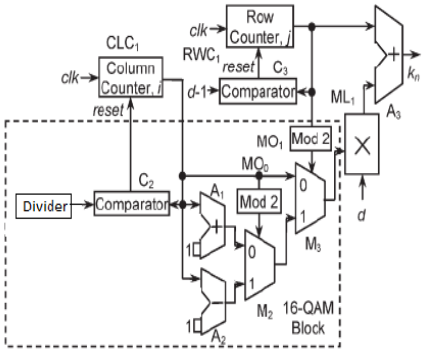
$$i' = (i+1)\%3\ and\ j' = j\%\ 3 \quad (30)$$

4. CIRCUIT TRANSFORMATION

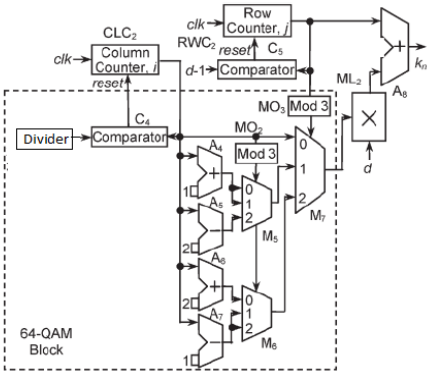
The transformation of the above algorithms to circuit is as shown in figure 3.



(a)



(b)



(c)

Figure 3: Hardware structure of the address generator (a)QPSK, (b)16 QAM, (c)64 QAM.

The top block consists of row counter, where clock is given as the input and RWC0 is used to generate row numbers between 0 to d-1. Now also in order to implement the permissible Ncbps, CLC0 is used with the help of clock input, multiplexer and comparator blocks to generate the variable column numbers.

When Ncbps is given as input, the total number of columns can be computed as Ncbps/d. Because of this, the column number will vary between 0 to (Ncbps/) -1. This technique can be obtained using divider block. For all modulation schemes and code rates used, the deinterleaver depth is given. With this, all the column numbers can be calculated which is given as input to the multiplexer. d X i is generated by using the multiplexer ML0 and d X i + j is generated using an adder A0. Which is the desired output to generate the address of QPSK [12].

The table column numbers calculated with manual computation for the permissible Ncbps values. When Ncbps is given as input, the total number of columns can be computed as Ncbps/d. Because of this, the column number will vary between 0 to (Ncbps/) -1. This technique can be obtained using divider and subtractor blocks. The inputs are given to the divider circuitry and the output obtained is subtracted by 1. These two operations together are done by divider circuitry.

5. EMBEDDED HARDWARE STRUCTURE

After looking at all the hardware structures that are discussed so far, some of the blocks used are in common in all the modulation schemes. So in order to reduce the space and hence the power, we can think of using the same blocks to embedded together and form a different overall top level circuit such that common blocks are shared between all the modulation schemes. i.e. multiplier, adder, row and column counters these are the same blocks we use in common. So while implementing the address generator for all these modulation schemes combinable commonly used blocks are shared. Figure 4 shows embedded hardware structure used to generate the address for all modulation schemes used.

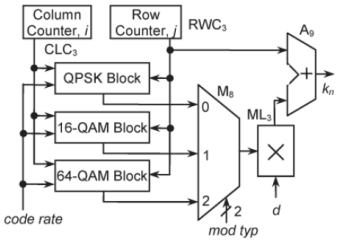


Figure 4: Embedded hardware structure used to generate the address for all modulation schemes used.

The incrementer/decrementer blocks used in QAM-16 can also be shared with that of QAM-64 i.e. the adder and subtractor. Such that we get the circuitry in a well-organized/optimized manner. So by this, QPSK, QAM-16 and QAM-64 blocks can be integrated. The second input to the multiplier and the comparator output varies for all the modulation schemes. So while integrating, by using the multiplexer M8, the desired output of column comparator and the second input to the multiplier are selected depending upon modulation scheme used.

6. SIMULATION RESULTS

The Simulation results of the proposed hardware of the address generator are implemented using Verilog Hardware Development Language on Xilinx ISE. Simulation results are obtained for QPSK,16-QAM and 64-QAM modulation types and for different code rates using Xilinx ISim are shown below in figure 5,6 and 7 respectively.

The figure 3 was modelled in Verilog and the simulated using Xilinx ISim and the deinterleaver address were successfully generated for different modulation schemes with varying code rates

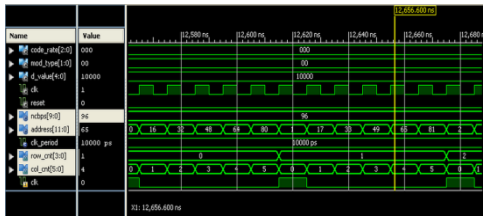


Figure 5: Simulation results for QPSK Address

The code rates were selected using the signal code rate, and the modulation scheme was selected using mode type signal. The deinterleaver addresses are generated on the waveform by kn. The simulated waveforms for the QPSK and QAM schemes are shown.

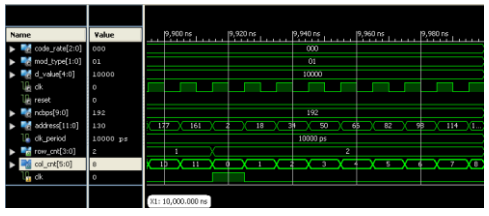


Figure 6: Simulation results for 16- QAM Address

The mode type is set to '0' to obtain the QPSK address and set to '1' to obtain the 16-QAM address, these values are shown in figure 5 and figure 6 respectively.

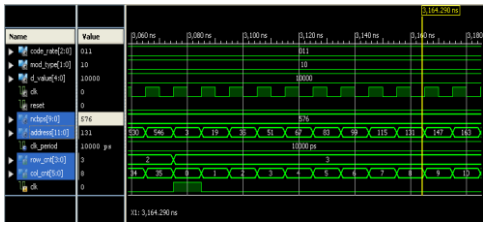


Figure 7: Simulation results for 64- QAM Address

In figure 7 the simulated waveform for the 64-QAM is shown, the values after the cursor in figure 5 to figure 7 shows the second row values for the different modulation schemes correspondingly. For obtaining the 64-QAM modulation scheme deinterleaved addresses value of signal mode type is set to '2' based upon which deinterleaver addresses are produced on signal kn as seen in figure 7.

7. DEVICE UTILIZATION SUMMARY

The Verilog HDL developed for the proposed WiMAX deinterleaver address generator is downloaded on Xilinx. Spartan-3 (Device X3CS400) FPGA [14].

Table 2: Synthesis report of HDL- Device utilization summary

Number of Slices	65 out of 3584	1%
Number of Slice Flip Flops	16 out of 7168	0%
Number of 4 input LUTs	120 out of 7168	1%
Number of IOs	31	
Number of bonded IOBs	27 out of 141	19%
Number of MULT18X18s	1 out of 16	6%
Number of GCLKs	1 out of 8	12%

There is a significant reduction in the FPGA Parameters like slices, flip flop and 4 input LUT's. Even there is a significant improvement in the operating frequency of this design when compared with LUT based technique is shown in Table 3.

Table 3: Comparison of results with the base paper versus LUT based technique

FPGA Parameters	Proposed Technique	Base Paper	LUT Based Technique
Slices	1%	3.49%	17.66%
Flip Flops	0%	0.50%	0.78%
4 Input LUT's	1%	3.35%	17.15%
Operating Freq	132.39 MHz	121.82 MHz	62.51 MHz

The IEEE standard defines the various interleaver depths and allowed code rates for WiMAX system [7] which is shown in table 1 and the deinterleaver addresses which are produced are shown in table 4. The addresses are obtained by using verilog to model equations respectively [4].

Based upon a new correlation developed which is described in the fig 4, this design is converted into corresponding hardware replicas and then it was modeled using Verilog The design was able to produce the deinterleaver addresses with all the code rates and modulation schemes as specified by the IEEE standard [5].

Table 4: Deinterleaver Sample addresses for different code rates

N_{cbps}, code rate and modulation type	De-interleaver addresses				
N_{cbps} = 96-bits, ½ code rate, QPSK	0	16	32	48	64
	1	17	33	49	65
	2	18	34	50	66
	3	19	35	51	67
N_{cbps} = 192-bits, ½ code rate, 16-QAM	0	16	32	48	64
	17	1	49	33	81
	2	18	34	50	66
	19	3	51	35	83
N_{cbps} = 576-bits, ¾ code rate, 64-QAM	0	16	32	48	64
	17	33	1	65	81
	34	2	18	82	50
	3	19	35	51	67

8. CONCLUSION AND FUTURE WORK

This work proposes a novel algorithm which replaces the utilization of floor function in WiMAX deinterleaver supporting QPSK, 16-QAM and 64-QAM modulation strategies and all conceivable code rates right now 802.16e. Region and postponement effective hardware of producing location for 2-D WiMAX deinterleaver without utilizing the floor function for all allowable code rates and three distinctive modulations are executed utilizing Xilinx Field Programmable Gate Array (FPGA) without manual processing's for aggregate number of segments. Henceforth by this, a straightforward, novel proficient asset usage with low power method is been accomplished with palatable results. The enhanced advanced circuit from our proposed algorithm is executed utilizing verilog. Examination of our proposed work with a LUT based system furthermore with a late work show noteworthy change on asset use and operating frequency.

In continuation to this work, further research should be possible in the zone of physical implementation, programmability, enhancing the memory sub-system dividing, more speed and applications. Where, as far as speed, distinctive modulation plan can be utilized like QAM=128/256 and so forth and subsequently additionally working recurrence can likewise be reachable and regarding applications, WiMAX can likewise be made utilized for portable applications where as a part of the proposed work done in this undertaking is been confined to non-convey capable gadgets.

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