Digital Library Creation using Standard Cells Implemented using GPDK 180 nm Technology

Physical VLSI Design of Digital Circuits

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ABSTRACT
Physical design in VLSI circuits is getting more complex with increase in circuit complexity. The major troublesome job in physical design is the difficulties encountered in routing. In physical design of digital circuits optimization of area is more important unlike in analog circuits where performance is given more priority. In the process of optimization of area in digital circuits routing in higher blocks can get more sophisticated. Standard cells are used as leaf cells in designing of higher digital blocks where the height of the standard cells has to be optimum. Therefore it is necessary to carefully design the standard cells and also create an environment for easy creation of bigger blocks using these leaf cells with simple routing at the top level. In this paper, a standard cell library is created where the height of the cells is optimized and also there are well defined space defined for systematic routing. Using these cells bigger digital blocks is created which demonstrates that routing can be made simple at the top level. In VLSI front end design parameters like gain, bandwidth, voltage swing etc are considered as major constraints [8]. In case of physical design of VLSI circuit's area, pin placement, routing, power planning and the shape of the layouts are the design constraints. In this paper, rectangular shapes for the leaf cells are created and the area of every standard cell is optimized. This helps in creation of digital circuits where one can access the created library and use the leaf cells as instance hence saving the design time. Routing is simplified by defining tracks on which metals will be routed. Tracks are designed such that any two metals can be routed on horizontal tracks placed one below other without the need to check of DRC rules. This is ensured by pre-defining the tracks and placing them at minimum DRC space defined by the technology used. All the digital circuits are implemented using cmos technology and the pmos and nmos devices widths are selected such that they are both of equal strength. This also ensures equal rise and fall time. All circuits are simulated using spectre tool and physical designs are verified for DRC and LVS.

General Terms
Cmos vlsi design, Physical design of digital circuits.

Keywords
Standard cell library, physical vlsi design, cmos technology, DRC (design rule check), LVS (layout versus schematic).

1. INTRODUCTION
The increasing demand for electronic devices which are reliable, low power consuming, processing at high speed and portable demands evolution in Integrated circuit technology, where the large number of transistors that can be integrated on a single according to Moore's law. To meet the demand for high performance processors, all the functionalities must be present on a single chip, which is a challenge for the design engineers. To make this task easier, CAD tools use ASIC libraries which consists of basic building blocks like logic gates, flip flops, mux etc., which are based on standard cell design techniques. Using these library components in physical design of the device reduces the time needed for implementation.

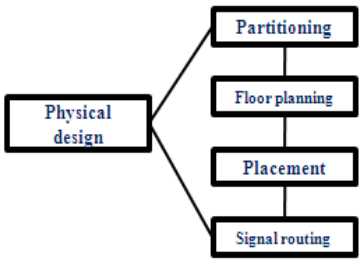

Fig 1: Physical design flow

The physical design is a process where all the components are mapped into a physical layout. The major design constraint of this design process is to get the minimum layout area and efficient interconnection between the sub-blocks to provide correct functionality and greater performance. The physical design flow for ASIC based design is shown in fig 1[9].

1.1 Partitioning
Larger circuits are partitioned into several smaller blocks due to its complexity. It becomes complex to layout the entire chip in single step and is a time consuming process. Designs without partitioning are difficult to debug, hence partitioning process involves dividing chip into several blocks. Any errors or bugs which are present can be addressed and resolved at lower level of hierarchies and debugging gets much simpler.

1.2 Floor planning and placement
This phase of physical design focuses on placement of set of rectangular areas which are to be fabricated on the chip. This phase deals with assigning location of all blocks and shapes to each flexible block. The goal of floor planning is to minimize the total area of chip which includes area of component and area for interconnect [6]. Floor planning of any physical design has to consider pin position, power routing and the overall shape of the layout. Placement of blocks is dependent on interconnection between blocks and the allowable routing delay. Blocks which communicate with each other are placed closer to reduce delay. Power planning is also critical issue

and by using a single access point for power can cause ground bounce which has to be avoided. Power planning is usually done in the form of a mesh and there are multiple taps for power supply to avoid ground bounce problems.

1.3 Routing

Based on logical arrangements of all blocks, physical connections are to be done. This process which involves creating physical connections is the routing process. Timing and signal integrity are important parameters to be considered for this phase of design. It is divided into global and detailed routing. In global routing nets are assigned to specific metal layers and in detailed routing, all the DRC rules are checked. Routing paths must be made as small as possible failing which there will be larger delay. Routing hence is a process whose complexity can be reduced in the floor-planning stage. In case of analog circuit designs delay will be a performance parameter which cannot be compromised and hence requires strategic floor-planning.

1.4 Standard cell design

Standard cells are gate level physical designs optimized for area. With shrinking size of the transistors and increase in the complexity of the circuits routing delay has become more critical for ASIC design. Accuracy of standard cell library will impact the ASIC design of the complete block. Hence care has to be taken in designing standard cells to minimize routing delays. There are different ways to route two metals and in standard cells routing on tracks is followed where space between the tracks is the distance between two vias. Height of the cells is decided based on the widths of the VDD/VSS power supply, pmos/nmos width and routing space. Usually the widths of power rails are wider as they have to supply current to all the sub-blocks and also must have least resistance path. With recent improvement in fabrication technology there are more than 6 levels of metal available for routing. Physical design of cells must use lower level metals like metal-1 and metal-2 as much as possible and utilize the higher level metals at the top levels. If the design cannot be done with just metal-1 then care has to be taken to use minimum routing of metal-2 and higher metals. With recent improvement in fabrication technology there are more than 6 levels of metal available for routing. This greatly impacts the top level routing in ASIC design. A good layout of the cell must have geometrical regularity which leads to uniform electrical characteristics. Every design of a cell must make sure if there is a possibility of drain/source sharing to reduce parasitic capacitance. Transistor sizing must be such that the pmos pull up strength and the nmos pull down strength are almost the same.

2. STANDARD CELL LIBRARY CREATION

Standard cells are custom designed physical layouts created for digital circuits. A standard cell also called as a leaf cell is a basic building block for higher blocks which can be built using these leaf cells are an instance. In paper [1] and [10] methodology for creating standard cells is given where layouts for standard cells are created for different drive strengths. Physical VLSI layout design concentrates on least silicon area usage on the chip with minimum complexity in routing. To create layouts with minimum area it is necessary to first set a standard cell height which is optimum. Routing is a major problem which has to be addressed in physical design and it becomes a tedious job as the circuit complexity increases. To avoid this complexity and to create an environment where routing can be done on tracks a grid based routing is used. A grid is layer created to define routing tracks which takes care of regular routing and avoids the DRC issues encountered in larger physical layouts. Fig 2.1.a and 2.1.b shows the grid layout created using hilite layer and tracks respectively. Tracks in a grid are placed at minimum distance such that any metal which are routed on these tracks will not produce errors by the DRC tools. The standard cell height can be decided by manually placing the VDD and VSS metals of a predefined width along with pmos and nmos device on a layout editor like virtuoso by cadence as shown in fig2.2.

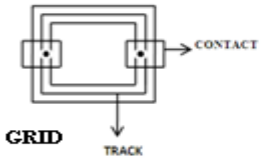

Fig 2.1.a: Grid design

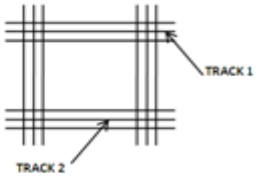

Fig 2.1.b: Tracks design

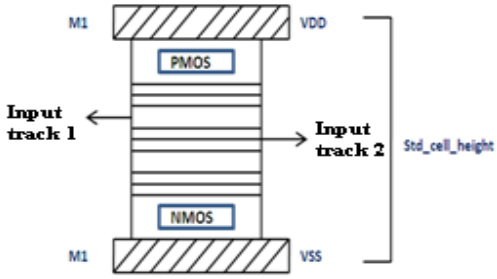

Fig 2.2: Standard cell height

It can be noticed that there are predefined tracks for input, outputs, VDD, VSS, pmos and nmos in the standard cell. This arrangement of routing on predefined tracks avoids the complexity in routing and also helps to create regular structured layouts. Layouts of every basic gates used in the design is created with the fixed standard cell height and the layout is allowed to grow horizontally. Due to this fixed defined height higher blocks like half adder, full adder, etc are created by abutting the basic gate layouts. Instances of the basic gates are used and abutted to create higher blocks [5]. It is up to the designer to grow the layouts horizontally or vertically as show in the fig 2.3. This can be a top level layout issue where the top level area and the shape is one of the criteria.

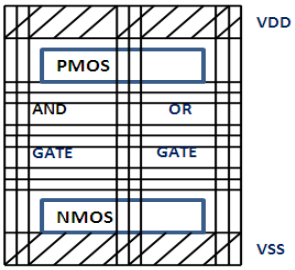

Fig 2.3: Higher blocks design using leaf cells

In a cmos based circuit design the bulk of every pmos and nmos device will have to connect to VDD and VSS power supply respectively. In digital design the pmos bulk will always be connected the highest voltage level in the circuit

(VDD) and the nmos bulk will be connected to lowest voltage level of the circuit (VSS). This ensures that there is no back gate effect and avoids the creation of secondary gate leading to leakage. All the pmos devices are placed in a nwell and this bulk has to be connected to VDD power supply. Similarly all nmos devices are places in p-substrate and this has to be connected to VSS power supply. Layout complexity can be reduced by creating a tap cell where the pmos bulk is connected to VDD and nmos bulk to VSS respectively. Whenever there is a need to provide the bulk connections for the mosfets, tap cell instance can be used hence reducing the design time. Figure 2.4 shows the tap cell design for a cmos based physical design. The height of the tap cell layout will also be set to the same standard cell height leading to regular bulk connection.

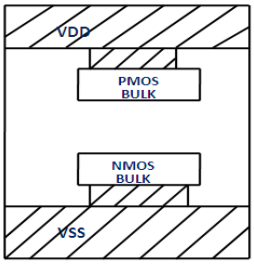

Fig 2.4: Tap cell design

3. DIGITAL CIRCUIT DESIGN USING STANDARD CELLS

Once the standard cell layouts for the basic gates are completed, physical layouts for any digital circuit are created by abutting the basic gate by using them as an instance [3][4] . Some circuits can be implemented by using transmission gates which uses less mosfets as compared to design using basic gates. In this paper, the design of combinational circuit like mux and sequential circuit like D-flip flop are illustrated. A 2:1 multiplexer circuit can be realized by using basic gates like NOT, AND and OR gates. The same mux circuit can also be realized by using transmission gates in which instance of any gates is not used. When abutting of layouts is done to create higher blocks VDD and VSS metals are overlapped to save the area wastage further. In the horizontal directions abutting must be done with tracks as the reference. Right most vertical track of a cell must overlap with the left most vertical track of other cell. This must be followed for abutting of layouts in both directions horizontally i.e. on right as well as to the left. Fig 3.1 shows how higher blocks are designed without wastage of silicon area and proper abutting in all directions [2]. It can be noticed from the fig 3.1 that overlapping of supply rails can reduce area and also regularity of layouts are maintained by systematic creation of higher blocks and without altering the tracks in both horizontal and vertical directions. At the top level all the supply rails are shorted together using higher level metals available in the technology. This routing of power can be done on top of the layouts by creating a mesh of power rails which joins all VDD supply together and also VSS supply. Designer has to carefully study the gate level netlist from the schematic and build the layouts such that the routing can be minimized along with minimum area utilization. Addition delay can be added with long routes depending on the block placements which must be reduced as much as possible.

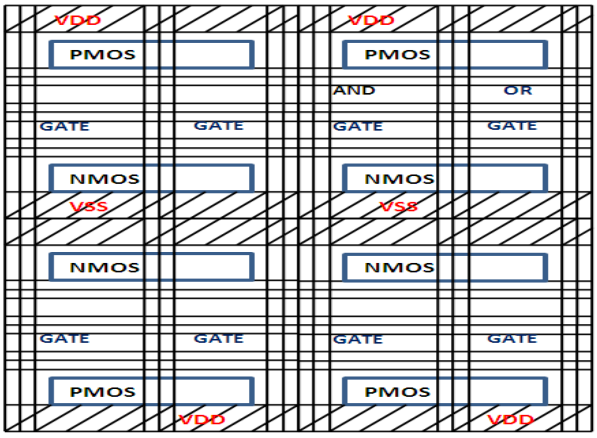

Fig 3.1: Abutting of leaf cells

Polysilicon layer used for gate terminals of mosfets are of high resistance than metal layers. If there are connections in the physical design where gate terminals of two mosfets are to be shorted together then poly routing must be avoided and instead metals must be used to avoid RC delay due to poly resistance.

4. DESIGN IMPLEMENTATION AND RESTULT ANALYSIS

Schematic entry for all the designs is done with composer schematic tool by cadence. Transistor sizing is done to equalize the rise and falls times of all cmos based gates [7]. Before the physical layout creation all the gates and higher block circuits simulation was carried out using spectre tool. Transient analysis for all the designs were done and major design parameters like power and delay was calculated. Physical layout creation was done using virtuoso-Layout XL tool by cadence. Grid was initially designed such that the any two tracks on the grid will have minimum DRC distance as per the GPDK technology. Using this grid layout standard cell was designed by placing instances of grid, pmos, nmos and supply rails as explained in section II. Fig 4.1 shows the layouts for standard cell height and tap cell. Once the cell height is fixed, all the blocks will has to be designed with the same height. It can be noticed that the tap cell is of the same height as that of the standard cell height layout. In the design the cell height is of 12µm considering the prepositioned place for pmos , nmos , input track and output track. Tap cell layout has the bulk of pmos as well as nmos bulk already connected to the supply rails VDD and VSS respectively.

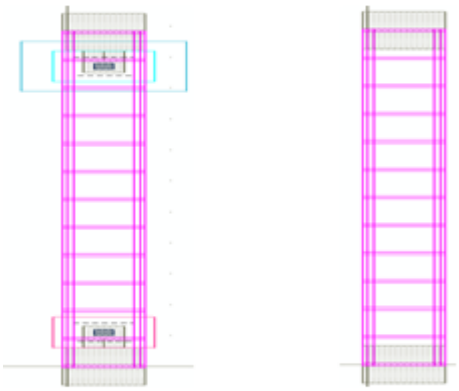

Fig 4.1: standard cell height and tap cell layout

Basic gates physical design was created using the standard cell height and tap cell layouts. All routings are done only on

the tracks only with lower level metal. Fig 4.2 shows the cell design for NOT gate and XOR gate with tracks positions for inputs and output mentioned. Tap cell is then abutted to the layouts to check for DRC and LVS verification, once the design is error free the tap cell instance is removed. This is done to save area which is consumed by the tap cell and this connection can be done in the top level design. Pmos and nmos devices require bulk connections within 10µm and hence a tap cell is not necessary for the basic gates in this level of hierarchy.

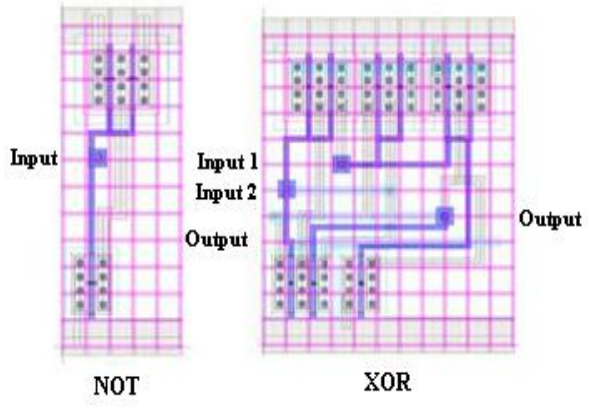

Fig 4.2: layout for NOT gate and XOR gate

All basic gates were designed on similar lines following the grid based routing and metal direction conventions as discussed in the chapter I. GPDK technology has 6 metal layers and for gate level design only lower metal layers i.e metal-1 an metal-2 were used. Fig 4.3 shows the layouts design for AND gate and NAND gate with the tap cell placed at the right. This is to illustrate the abutting of tap cell to the layouts for bulk connections.

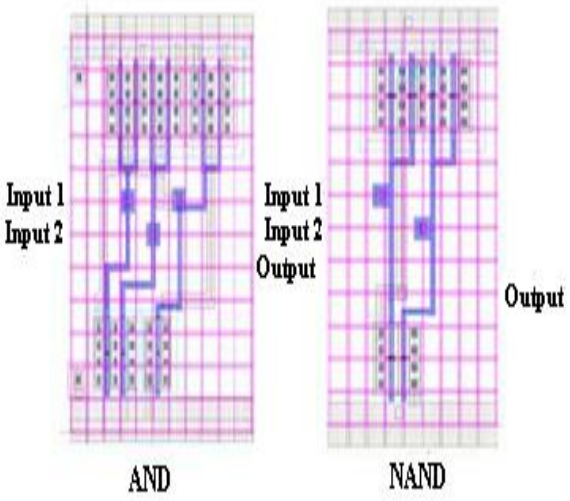

Fig 4.3: AND gate and NAND gate layout

Other combinational circuits like MUX and TG were designed. Multiplexer was realized using transmission gate using less number of mosfets as shown in figure 4.4

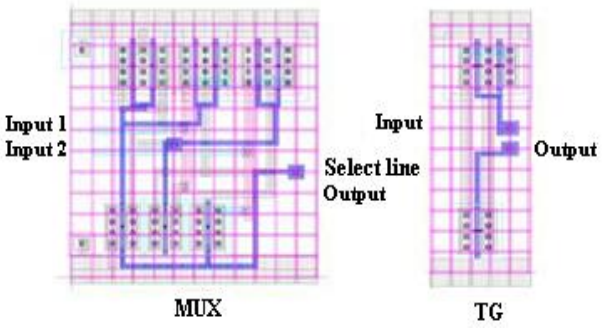

Fig 4.4: MUX gate and TG layout

Sequential circuits will use flip flops and latches as storage devices. Most of the real time circuits will need storage of data for processing the previous data. D flip flop is the basic building block for most of the sequential circuits. Hence there is a need to optimize the device for area in physical design. In this paper, D- flip flop design is based on universal NAND gate and with transmission gate. Fig 4.5 shows the layout for NAND gate based flip flop.

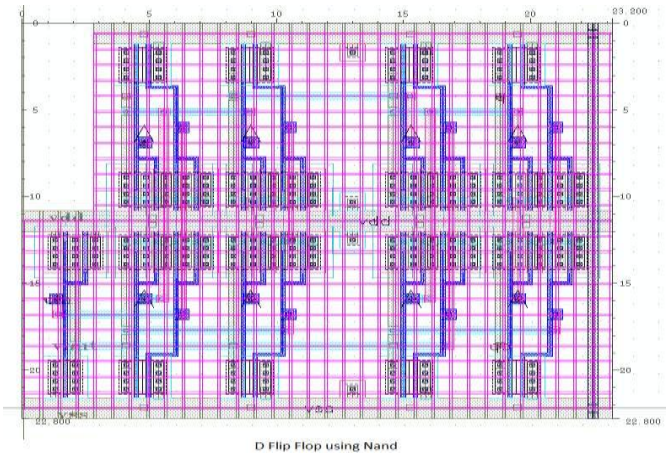

Fig 4.5: D-Flip flop using NAND gate

It was observed that the design using NAND gate consumed more silicon area. Hence architecture for D-FF using less area was designed using transmission gates. It can be observed there is an empty space for the flip flop but this will be compensated in the top level layouts where these L-shaped layouts can be abutted to give rectangular layouts with no empty spaces. Fig 4.6 shows the layout design for TG based D-FF.

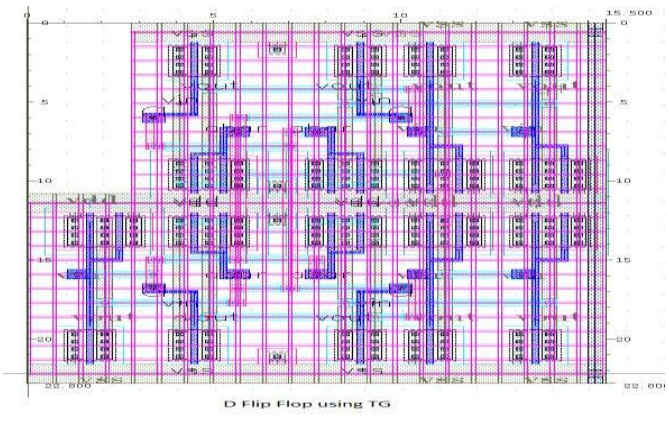

Fig 4.6: D-Flip flop using TG

All the layouts were verified for DRC and LVS verification using ASSURA tool. Area utilized by the layouts was measured for each design. Table 4.1 shows the delay, power consumption and area utilization details for all the blocks in library. Table 4.1 shows the area reduction for the D_FF using TG from 528µm2 to 353µm2 reducing the overall area by approximately 33%. Design of D-ff reveals the advantages of track based routing showing simple routing for complex designs. Tap cell are placed only when it is necessary for every 10µm distance from the devices as shown in fig 4.5 and 4.6.

Table 4.1. Delay, area and power consumption of gates and blocks

Cell type	Cell name	Power in watts	Delay in seconds	Area in Sq. m
Basic gates	AND gate	573.4n	202.4n	91.77 µ
Universal gates	NAND gate	395.3 n	400.2 n	68.4 µ
	Nor gate	942.5n	400.1n	64.1 µ
Derivative of basic gate	XOR gate	800.3 n	402.4 n	102.96 µ
Combinational circuits	Half adder	1.363 µ	202.4 n	190.63 µ
	Full adder	4.223 µ	503n	587.12 µ
	MUX	839n	704n	110.01 µ
Sequential cells	D flip flop using TG	2.47 µ	153.3 n	353.4 µ
	D flip flop using NAND gate	5.89 µ	153.2 n	528.96 µ

5. CONCLUSION

This paper proposes a novel routing techniques for physical design of digital circuits. Using these techniques a library is created which consists of basic gates and few digital circuits. Design time and routing complexities has been reduced by regular metal routes for all designs. Silicon area wastage is reduced wherever possible in every design. A library is created with basic gate, combinational circuits and sequential devices like flip flops. This library can be used to save time in the higher block design if the design meets the required constraints of the designer. This library can further be improved by adding more blocks which can be used for building bigger blocks. Basic gates with different strengths can be added to which can be utilized for different specifications. Back annotation and characterization of all the cells can be done as part of future work.

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