Multiplexer based Design for Ternary Logic Circuits

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ABSTRACT
Three valued logic which is also called as a ternary logic is a best alternative to conventional binary logic. Ternary logic has got its own importance due to its energy efficiency resulting from reduced complexity of interconnect and chip area. This paper presents a methodology for the design of ternary multiplexer circuit and also the design of ternary logic circuits based on CMOS. Designing of ternary multiplexer is presented first. Later the proposed methodology for the design of ternary logic circuits is presented. This proposed design methodology is used to implement 1-bit half adder circuit using SPICE model. These new proposed implementations are compared with the old existing designs for the parameters like delay, power, number of transistors, power delay product etc. Simulation results indicate that the mux based 1-bit half adder design has reduced number of transistors, delay and power delay product when compared to the existing binary logic design.

Keywords
MOSFET's, Ternary Logic, Ternary Multiplexer**.**

1. INTRODUCTION
Traditionally digital computation is performed on two valued logic also called binary logic. Multi-valued logic (MVL) replaces the classical characterization of variables with more than two values. One example of multi-valued logic is Ternary Logic. Ternary logic has got its own importance due to its energy efficiency resulting from reduced complexity of interconnect and chip area [1][2]. Research on [3] design of ternary logic using CMOS is going on. It has been shown that the performance of CMOS technologies can be enhanced by adding MVL blocks to binary ICs .There are two kinds of MVL circuits which are based on MOS technology. One is current mode MVL circuit and the other is voltage mode MVL circuit. Voltage mode MVL is achieved by multi-threshold CMOS design. Multiple threshold values in CMOS can be achieved by using different bias voltages to the bulk terminal of the transistors.

The another type of Field Effect Transistor available whose Gate input is electrically insulated from the main current carrying channel and is therefore called an **Insulated Gate Field Effect Transistor** or IGFET. The most common type of insulated gate FET which is used in many different types of electronic circuits is called the **Metal Oxide Semiconductor Field Effect Transistor or MOSFET** for short**.**

MOSFETs are three terminal devices with a Gate, Drain and Source and both P-channel (PMOS) and N-channel (NMOS) MOSFETs are available[5]. The main difference this time is that MOSFETs are available in two basic forms:

1. Depletion Type – here the transistor requires the Gate-Source voltage, (V_{GS}) to switch the device "OFF". The depletion mode MOSFET is equivalent to a "Normally Closed" switch.
2. Enhancement Type – here the transistor requires a Gate-Source voltage, (V_{GS}) to switch the device "ON". The enhancement mode MOSFET is equivalent to a "Normally Open" switch.

MOSFET devices are especially valuable as electronic switches or to make the logic gates because with no bias these MOSFET's are normally non-conducting and this high gate input resistance means that very little or no control current is needed as MOSFETs are voltage controlled devices. Both the P-channel and the N-channel MOSFETs are available in two basic forms, the Enhancement type and the Depletion type.

1.1 Ternary Logic
Three valued logic which is also called as a ternary logic is a best alternative to conventional binary logic. Ternary logic has got its own importance due to its energy efficiency resulting from reduced complexity of interconnect and chip area. Ternary logic provides best utilization of the transmission channels because of the more information content carried by each line, also gives more efficient error detection and correction codes and possess potentially higher density of information storage. If the ternary logic is employed then the arithmetic operations can be carried out faster. If we employ the ternary logic the main advantage is that we can reduce the number of required computation steps. Because each signal will have three different values, the number of digits required in a binary logic is log32 times more than the ternary logic. Ternary logic gates require less number of gates and hence they are the good candidates for the decoding blocks. Whereas binary logic gates are good for fast computation modules.

Let a system be L whose elements called propositions or statements are valued in the set {0, 1, 2} which is denoted by Z3. If X is a proposition, the value of X can be seen as a

$$V : L \rightarrow \{0, 1, 2\}$$

Such that

$$V(X) = \begin{cases} 2 & \text{if X is true} \\ 1 & \text{if X is intermediate} \\ 0 & \text{if X is false} \end{cases}$$

Ternary logic has the logic levels '0' which means logic-0 or low voltage in binary. Logic '1' means an intermediate stage or meta stable state and '2' means logic-1 or high voltage in binary. The meta stable state can be thought of as either true or false. In realizing combinational and sequential logic functions ternary logic acts as basic building block.

Here ternary-gates are implemented using MOSFET's as basic switching elements, and this is referred as T-Gates. These ternary gates qualify as a universal element in several

different senses. Compared with ordinary algebra, the Post and Modular algebra has several advantages available for the design of ternary switching functions.

The basic operations of ternary logic is as follows, Ternary Inverter

$$STI = \overline{X^1} = 2 - X$$

$$PTI \text{ , } NTI = \overline{X^i} = \begin{cases} i & \text{if } X \neq i \\ 2 - i & \text{if } X = i \end{cases}$$

where the minus sign represents arithmetic subtraction. for the NTI operator. The

Ternary AND and Ternary OR gates

$$X1 \cdot X2 \cdot \ldots \cdot Xn = MIN(X1, X2, \ldots, Xn) \quad (2)$$

$$X1+X2+\ldots\ldots+Xn=MAX(X1,X2,\ldots.Xn) \quad (3)$$

Where (1), (2) and (3) indicate OR, AND and NOT operations respectively for ternary logic

Table 1: Function Table for Ternary Inverter

X	$\overline{X^0}$ (NTI)	$\overline{X^2}$ (PTI)	$\overline{X^1}$ (STI)
0	2	2	2
1	0	2	1
2	0	0	0

2. EXISTING SYSTEM

The existing design methodology can be divided in to three stages. In the first stage a ternary decoder, which is a one input 3-output combinational circuit, is used to generate mutually exclusive unary functions for an input x. The response of ternary decoder to the input x is given

$$X_k = \begin{cases} 2, & if\ x = k \\ 0, & if\ x \neq k \end{cases}$$

Where, k can take logic values of 0, 1 and 2, corresponding to voltages0, 2.5 and 5V respectively. The decoder consists of a PTI gate, two NTI gates and a NOR gate.

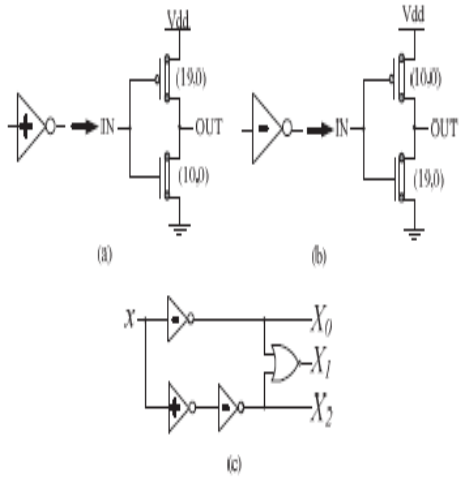

Fig 1: (a) PTI Gate (b) NTI Gate (c) Ternary Decoder

The design methodology of PTI shown in figure (a) and NTI inverter shown in (b). The numbers in the brackets across the MOSFETSs represent the chirality. The NOR gate that is used in the design of decoder is a simple binary logic gate (with logic levels 0 and 2) and can be designed by the MOSFETs in CMOS inverter design. The schematic of the ternary decoder is shown in figure (c). The outputs of the ternary decoders are combined according to the truth table using only ternary gates or both ternary and binary gates.

1-bit Ternary Half Adder.

The 1-bit half adder implementation is as shown in the figure 2. The T-buffer shown in the figure6.2 is a level shifter which converts logic 2 to logic 1. A 1-bit comparator, which can generate two signals indicating greater and equal, can also be designed using the same methodology.

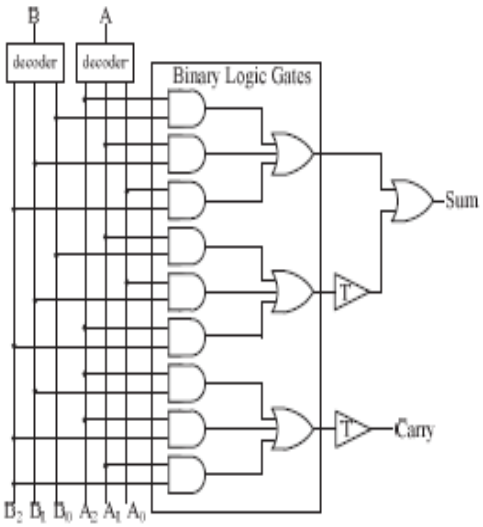

Fig 2: Existing Design of 1-bit Half Adder

3. PROPOSED SYSTEM

A Multiplexer based approach for design of ternary logic circuits is presented. Initially a design of transmission gate ternary multiplexer is presented and then design methodology using ternary multiplexer is presented.[11]

Ternary Multiplexer

A ternary multiplexer can be designed using a ternary decoder and three ternary 2-input AND gates. The design of ternary AND gate is complex. Hence a transmission gate based multiplexer can be designed. This multiplexer consists of three transmission gates, one ternary decoder and three simple inverters. Figure6.3 shows the implementation and representation of transmission gate based ternary multiplexer.

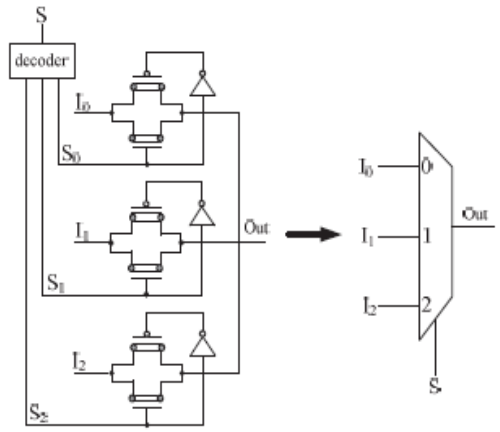

Fig 3: Transmission gate based Ternary Multiplexer

The operation of the ternary multiplexer is straightforward. When the select signal S is logic 0 the decoder output S0 will be logic 2 and the input I0 will be passed on to the output. Similarly if S is logic 1 I1 is passed to the output, if it is 2, I2 will be passed on to the output. This transmission gate based CNFET ternary multiplexer is used in the proposed methodology to design ternary logic circuits.

Proposed Multiplexer Based Design Methodology. 1-Bit Ternary Half Adder- A multiplexer or chain of multiplexers can be used to design any desired logic in the conventional binary logic which is predominantly used in the FPGA design. The same methodology can be used for designing ternary logic circuits. Consider for an example the truth table of a 1-bit half adder sum as shown in Figure 4.

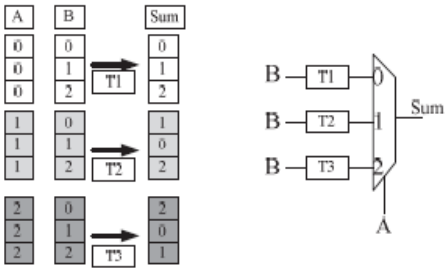

Fig 4: Half-Adder Sum Implementation

As seen from the truth table: When the operand *A* is 0, *B* (0, 1, 2) is to be transformed in to (0, 1, 2) to get the sum. Similarly when operand *A* is 1, *B* (0, 1, 2) is to be transformed in to (1, 0, 2). The transformation functions T1, T2 and T3 can be designed by using one more stage of multiplexers or by using optimized combination of binary and ternary gates. The choice depends on the complexity of the transformation. If the transformation of arbitrary input, *x* (0, 1, 2), results in output which has all the logic values, then the multiplexer implementation is better. This is due to the fact that the implementation of transformation using the ternary and binary gates consists of complex ternary OR gate. The transformation function T2 with B as input, which can be used in the half adder implementation is shown in figure 4. The OR gate with a· indicates that it is a ternary gate. The T-Buffer shown in figure 4 is a level shifter circuit.

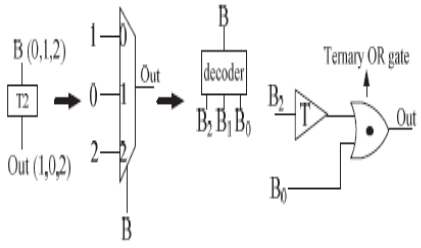

Fig 5: T2 transformation function Implementation

If the transformation of arbitrary input, *x* Consider a transformation function which transforms the input *x* (0, 1, 2) to output (0, 2, 2). The transformation function implementation for this case using multiplexer and ternary binary logic gates is shown in the figure 6. The implementation using ternary-binary gates consists of one NTI gate, and simple binary inverter gate which works on logic levels 0 and 2.

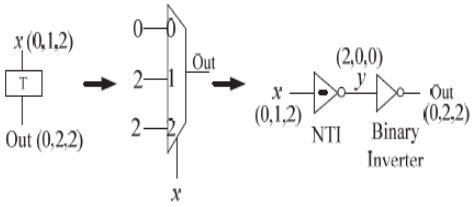

Fig 6: Example of (0,1,2) to (0,2,2) Transformation

The methodology explained above can be implemented for all the 27 possible transformation functions using both multiplexer implementation and binary-ternary gate implementation and the optimal implementation can be found. The ternary implementation of half adder circuit using the proposed methodology is shown in the figure 6. The proposed half adder sum implementation consists of three ternary multiplexers and sum implementation consists of one ternary multiplexer, one NTI gate, one binary inverter gate and a T Buffer. The half adder implementation also consists of two ternary decoders which are needed to generate the unary signals corresponding to the inputs *A* and *B.* The methodology presented above can be used implement any ternary logic circuit. The proposed multiplexer based methodology can also be used in the implementation of ternary logic based FPGA circuits. The challenge in such an implementation would be design of level restoring circuit after a chain of multiplexer gates

4. SIMULATION RESULT

Simulations on 1-bit half adder circuit, which are designed using existing as well as proposed design methodology, have been performed in TSPICE using the MOSFET model at 5V power supply. The AND-OR circuits in the existing 1-bit half adder implementation have been implemented optimally by transistor stacking. Table show the simulation result for 1-bit half adder implementations.

Table 2: comparison of power and delay of exisisting and proposed 1-bit ternary half adder respectively

1-bit Ternary Half Adder	Delay (s)	Power(W)	Power-Delay Product	No of Transistor
Existing System	8.69	1.288	1.5147	124
Proposed System	5.88	2.676	0.7833	44

5. CONCLUSION

A multiplexer based methodology for design of ternary logic circuits was presented. First a design of transmission gate based ternary multiplexer is presented. Then the methodology to design ternary logic circuits based on the ternary multiplexer is presented. This proposed design is used to implement 1-bit half adder circuits using SPICE model. These new proposed implementations are compared with the old existing designs for the parameters like delay, power, number of transistors, power delay product etc. Simulation results indicate that the mux based 1-bit half adder design has reduced number of transistors, delay and power delay product when compared to the existing binary logic design design**.**

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