A Novel n-bit Arithmetic Logic Unit Design based on Reversible Logic

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ABSTRACT
In this paper, the design of an N-bit reversible Arithmetic Logic Unit (ALU) is presented. In modern Era of circuit designing, complexity of circuit increases day by day. Hence power dissipation plays important role in designing of any digital circuit. There are two types of power losses, leakage power and dynamic. Reversible logic design can also be used for same objective reversible gates are used which have equal number of inputs and outputs. This research has focused on reducing dynamic power dissipation by reversible logic design which provides substantial reduction in dynamic power dissipation (~50% reduction is observed). The later design is found advantageous over the former irreversible designs in terms of power dissipation.

Keywords
Reversible logic, ancilla input, garbage output,dynamic power

1. INTRODUCTION
Applicability of the Moore's Law is impractical in current decades. As the digital systems are being built faster and complex, more research concentration must be given towards power dissipation of CMOS circuits. In microelectronics, Reversible's are circuits (gates) that have the same number of inputs and outputs and there happens to be a one-to-one mapping between inputs and outputs. Thus the vector of input states can be always uniquely reconstructed from the vector of output states. Because truly low power circuits cannot be built without the concepts of reversible logic, various technologies and circuits for reversible logic are recently being studied. Landauer [1] proved that power loss is an integral feature of irreversible circuits that have information loss irrespective of the technology the circuit is implemented in. Also, Bennett [2] showed that in order to keep a circuit from dissipating any power, it had to be composed of reversible gates.

ALU is a combinational logic circuit which allows a computer to do basic logical operations such as AND, OR etc, therefore included in every CPU. An ALU has one or more inputs and only one output which are dependent only on inputs applied at that instant as a function of time and not on past condition. To implement the logic the constant input provided are called ancilla inputs. In order to maintain the reversibility the unused output is termed as garbage output. In past few years research work has been done on reversible ALU [3][5][7]. The good design approach is to minimize the garbage outputs. Reversible logic is a core part of the quantum circuit model.

1.1 Definition1
For an *n* input/output logic gate, if there is a one-to-one correspondence between its inputs and outputs, then this logic gate is reversible.

$$I_i = (I1, I2, I3,\ldots\ldots\ldots\ldots I_n)$$

$$O_o = (O1, O_2, O_3,\ldots\ldots\ldots On)$$

Where the input is vector, and is the output vector. That is to say, a reversible gate has the same number of inputs and outputs. Commonly used reversible gates are NOT gate, CNOT gate, CCNOT gate (Toffoli gate), Fredkin gate and so on [8][9]. There is no loss of information bits for these gates.

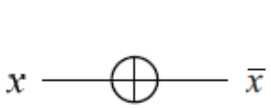

Figure1: Not gate

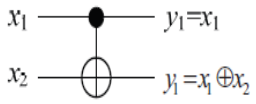

Figure2: CNOT gate

NOT gate is the only single-input single-output reversible logic gate, and its function is to make the information bit flip (Figure 1). CNOT gate has two inputs/outputs, and the first Input x1 is the control bit, the second one x2 is the target bit (Figure 2). It implements the logic functions: y1 = x1 and y2 = x1 xor x2. That is to say, when x1=1, y2=~x2 and with x1=0, y2=x2. Whether the value of target bit is inversed depends on the control bit. CCNOT gate has three inputs/outputs, and the first two inputs x1and x2are the control bits, the third one is the target bit (Figure 3). It implements the logic functions: It implements the logic functions: y1 = x1, y2 = x2, y3 = x1x2 xor x3. When x1 =x2 =1, one can get y3 = ~x3 in other cases y3 will remain equal to x3.So first two bits are controlling the output y3.

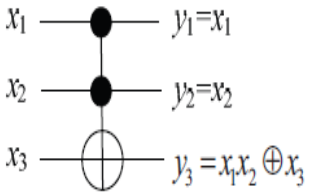

Figure 3: CCNOT gate

Definition 2: *n* -Toffoli gate has *n* intputs and n outputs, and the first (n-1) inputs are control bits, the n^{th} input is target bit (Figure 4). It also can be called the Toffoli gate series. It implements the logic: $y_1 = x_1$, $y_2 = x_2$, $y_3 = x_2$, ……,$y_{n-1} = x_{n-1}$, $y_1 = x_1$, $y_n = \sim x_n$,When $y_1 = x_1 x_2$,…. $x_{n-1} = 1.1.1\ldots.1$, we can get $y_n = \sim x_n$

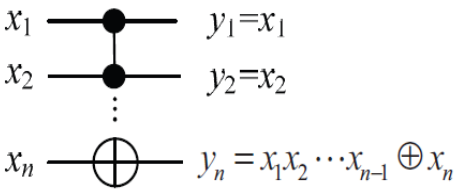

Figure 4: CCNOT gate

In figure (5) the basic reversible gates used in the design are shown

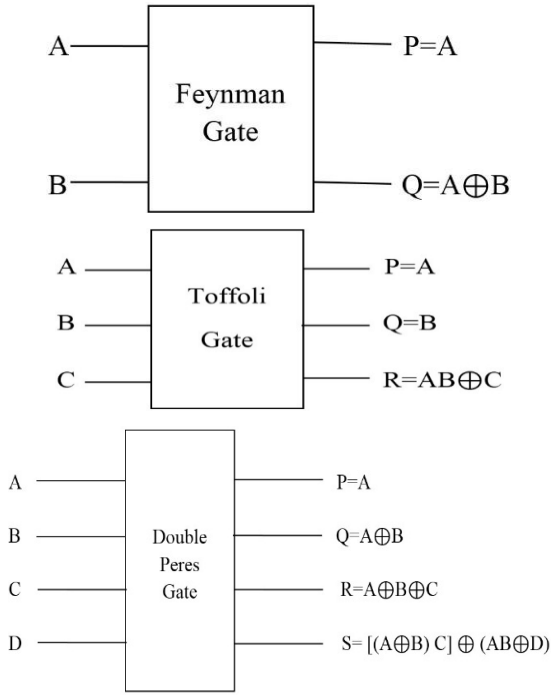

Figure 5: Basic Reversible gates

2. PURPOSED ARITHEMETIC LOGIC UNIT

2.1 Purposed ALU

The block diagram of purposed Arithmetic Logic Unit designed through reversible logic gates is shown in figure (6) composed of two unit viz. Arithmetic Unit and Logic Unit further output is given through 2:1 mux and output is given at fun. 16 bit inputs are given to A and B and output is taken from fun of 16 bit A 2:1 MUX is used for multiplexing Arithmetic unit and logic unit. Functions performed by this ALU are listed in the table

2.2 Arithmetic Unit

2.2.1 One Bit Arithmetic Unit

1bit purposed structure of Arithmetic unit is as shown in figure 7 composed of 3 Toffoli gates, one Feynman gate and one DPG gate is used. DPG gate is used as full adder and Toffoli gate with Feynman gate provide the control mechanism which gives various arithmetic functions. The single arithmetic unit have four ancilla input and 5 garbage outputs.

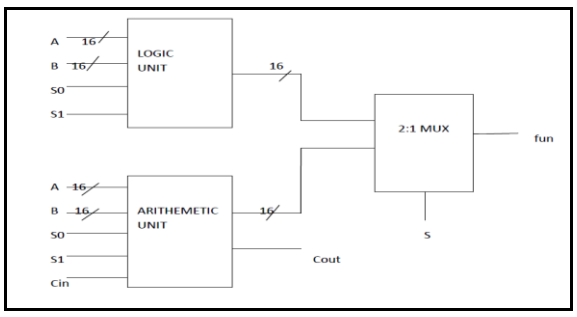

Figure 6: Block diagram of purposed ALU

The Boolean equation for the Arithmetic is:-

For DPG gate we have three inputs i.e A, Y1 and Cin so equation for Y1 is as follows

$Y1 = \bar{S}_0 (S1\bar{B} + \bar{S}_1 B) + S_0 S_1$

Sum = A ⊕ Y1 ⊕ Cin

$Cout = AY_1 + Y_1 Cin + ACin$

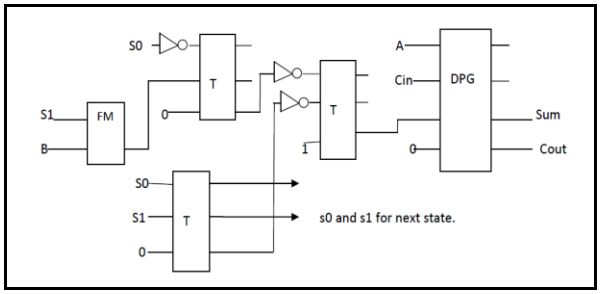

Figure 7: 1-bit arithmetic unit

2.2.2 One Bit logical Unit

1 bit logic unit is composed of two 4*4 Toffoli gate , one 3*3 and one 5*5 Toffoli gates and one Feynman gate is used for the logic structure this purposed as shown in figure 8 performs four basic logic operations viz. AND , OR , XOR and NOT .Boolean equation for the logic unit is

$Y = \bar{S}_1 (A\bar{B} + B\bar{A}) + \bar{S}_0 \bar{A}B + \bar{S}_0 S_1 A B$

This reversible logic unit has 4 ancilla inputs and 6 garbage output. It provides great reduction in the logic power in comparison to the irreversible logic unit.

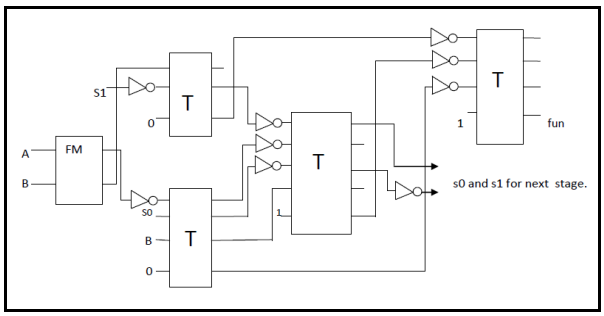

Figure 8: 1-bit logical unit

2.2.3 N-bit arithmetic unit

N bit purposed structure of Arithmetic Unit is obtained from single bit structure by propagating both select lines so,s1 and carry output to the next stage as shown in figure(9). The purposed N bit Arithmetic Unit have 4N ancilla inputs and 5N garbage outputs. For 16 bit ancilla inputs and garbage outputs will be 64 and 80 respectively.

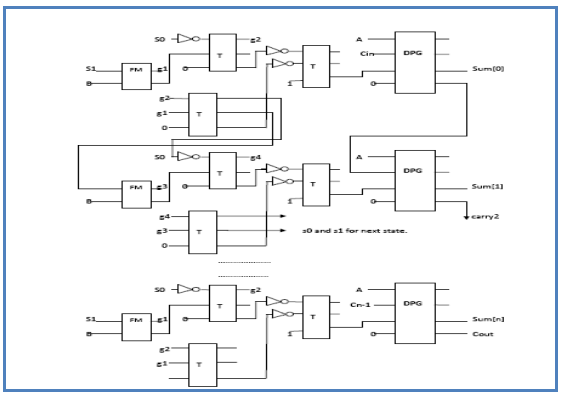

Figure 9: N-bit Arithmetic Unit

2.2.4 N-bit logic unit

N bit structure of the logic unit as shown in figure 10 can be obtained from the single bit reversible purposed structure by propagating the select lines so and s1.This n bit logic unit have 4N ancilla inputs i.e constant inputs and 7N garbage outputs. Total number of gates used for this design is 14 N. For 16 bit ancilla inputs and garbage outputs will be 64 and 112 respectively. Total number of gates for 16 bits will be 224.

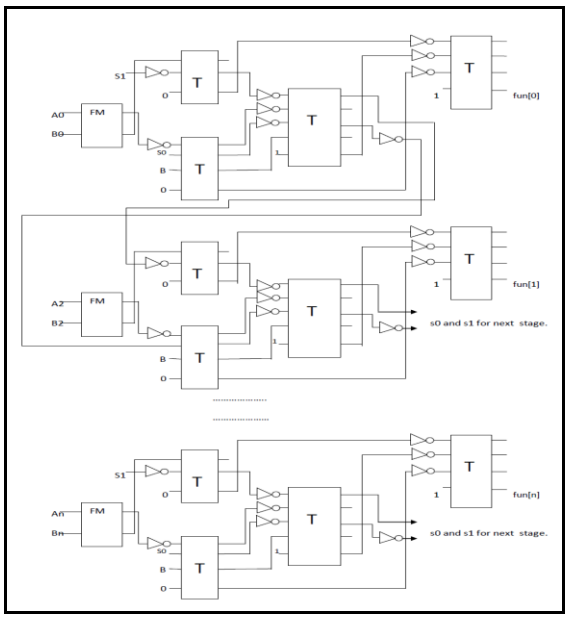

Figure 10: N-bit logic unit

2.2.5 Reversible MUX Design

2:1 MUX is used for combining the two unit viz. Arithmetic and logic unit together. Here MUX is realized is using three Toffoli gates as shown in figure 11 MUX equation is

OUT = A.S + B S bar

This MUX provide significant reduction in the power in comparison to irreversible MUX. It is used for multiplexing the Arithmetic unit and logic unit for making single unit i.e. Arithmetic Logic Unit. Figure represents the functional table 3 for the purposed reversible ALU.

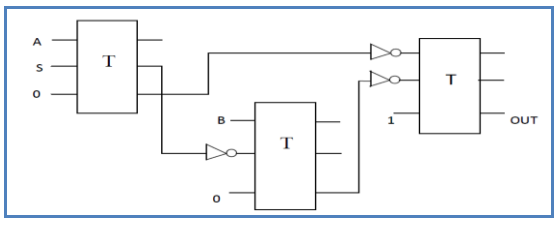

Figure 11: 2:1 Reversible MUX

This reversible mux have three ancilla inputs and five garbage outputs.

3. SIMULATION AND ANALYSIS

3.1 Simulation

In order to verify the functional correctness of our reversible ALU, we use ISE simulator to make the corresponding simulation. A and B are two 16 bit inputs and S, S0, S1 are select lines. Fun is the 16 bit output. Simulation of 16 bit reversible ALU is shown in figure 12 Post synthesis simulation is also done with which is same as the pre synthesis simulation.

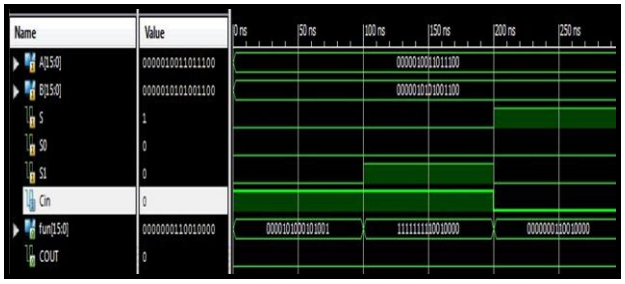

Figure 12: Simulation waveforms of 16 bit Reversible ALU

3.2 Power analysis

The Xilinx Power Analyzer can perform a power analysis at any time during the design cycle. Signal rate play a significant role in the power calculation it is defined as how many times that particular signal changes during clock period it is very critical for the designer to provide this for efficient power calculation. Reversible logic structures reduce the dynamic power consumption especially magical reduction in the logic power.

The important power components to consider include the following:

Static (standby) power: Static power is the amount of power the device consumes when it is powered-up but not actively performing any operation (i.e., the device is not clocked).

Dynamic (active) power: Dynamic power is the amount of power the device consumes when it is actively operating (i.e., the device is clocked).

Power analysis for 16 bit Reversible ALU: Total power for the 16 bit reversible ALU is the sum of device static power i.e. leakage power and dynamic power. Dynamic power is the sum of Input Output power, logic power and data power which shown in figure 13. It is reduced by 5.12 % in comparison to irreversible Arithmetic Logic Unit.

Input/output power: This is the power dissipation when the device is configured but there is no switching activity which is almost same for both types of ALU is 34.55 mW.

Data Power: Data power dissipation is due to the data switching. It is reduced by 41.6 % through reversible logic gates in comparison to 16 bit irreversible ALU which perform the same functionality .Data power for the 16 bit reversible ALU is 1.44 mW.

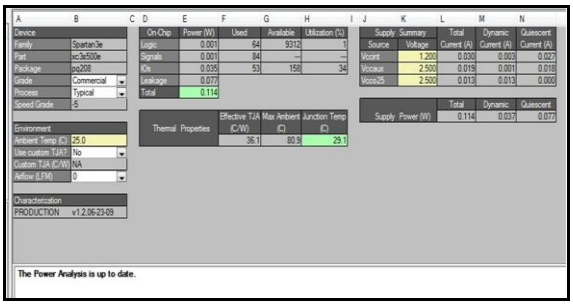

Figure13: Power dissipation for 16 bit reversible ALU

Logic Power: Logic power is the additional power consumption from the user logic utilization and switching activity also called design dynamic power. There is magical

reduction in the logic power consumption using reversible logic gates because of one to one correspondence between input and output which prevent the loss of bits. Logic power consumption is reduced by 50.6 % for 16 bit Arithmetic Logic Unit as shown in the table 1

Table1: Power dissipation comparison for 16 bit ALU

Source of power	16 Bit Irreversible ALU (mW)	16 Bit Reversible ALU (mW)
IO Power	34.55	34.55
Data Power	2.38	1.39
Logic Power	2.39	1.18
Total Power	39.0	37.0

Area comparison for ALU: Table 2 shows the area comparison between irreversible and reversible Arithmetic Logic Unit (ALU). The Area is reduced by 34% by using reversible Arithmetic Logic Unit.

Table2: for Area comparison of 16 bit ALU

Parameter	16 Bit Irreversible ALU	16 Bit Reversible ALU
No. of slices	52	34
No. of 4 I/P LUT	98	64
No. of Inputs	53	53

Table3: functional table for ALU

S	S0	S1	Cin	Fun
0	0	0	0	A+B
0	0	0	1	A+ B +1
0	0	1	0	A +B'
0	0	1	1	A – B
0	1	0	0	A
0	1	0	1	A + 1
0	1	1	0	A – 1
0	1	1	1	A
1	0	0	X	XOR
1	0	1	X	AND
1	1	0	X	OR
1	1	1	X	NOT

4. CONCLUSION

These new ALU designs are advantageous to irreversible ALU and favour low power dissipation and also consume less area which is desirable for realization of a reversible central processing unit. RTL coding is done in Verilog HDL and simulation is done with ISE Simulator. Synthesis is done with Xilinx 12.3. Power is estimated using XPower analyzers from which it is estimated the logic power and area is reduced by 50% and 34% respectively. Field Programmable Gate Array (FPGA) Spartan 3 is used for the hardware realization of the design. The results of the research can be exploited very effectively in quantum computing and low power design. The future scope of this research includes the applicability of Moore's law in the next few decades through the quantum computing using reversible logic. In quantum technology there are gates such as X (analogy of Boolean NOT), Z and Hadamard gate, which are all self-inverses. However, rotation gates are not self inverses. Synthesis procedures based on the truth table are limited to functions of 30 inputs (if usage of modern computers for CAD is expected). Thus, a new design procedure needed. The research may be useful to develop the synthesis procedures based on the function factorization and theory of the group of permutations.

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