All Optical Reversible NOR Gates using TOAD

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ABSTRACT
In recent past, reversible logic is emerged as a promising computing paradigm with applications in low-power CMOS, quantum computing, optical computing and nanotechnology. Optical logic gates become potential component to work at macroscopic (light pulses carry information), or quantum (single photon carries information) levels with high efficiency. In this paper, we propose a novel scheme of TOAD-based all optical reversible NOR gates and their universal application in all-optical domain. Simulation results verify the functionality of these TNOR and PNOR gates as well as reversibility.

Index Terms
Reversible logic gates, Terahertz Optical Asymmetric Demultiplexer (TOAD), TNOR gate, PNOR gate

1. INTRODUCTION
All-optical switching - the switching of one beam of light by another — is an essential operation for transparent fiber optic networks and for all forms of optical information processing [1-6]. To overcome the electronic bottlenecks and fully exploit the advantages of optical fiber communication, it is necessary to move towards networks where the transmitted data would remain exclusively in the optical domain without optical-electrical-optical (OEO) conversions [7-9]. Two fold driving forces for this all-optical switching are the broadband photonic network environment that emerges due to rapid convergence of telecommunication and informatics.

In conventional computers, majority of the computation operations are irreversible i.e. once a logic block generates the output bits based on certain input combinations, the later bits are lost. The classical set of gates such as AND, OR and X-OR are irreversible as they are all multiple-input single output logic gates. However, this is not the case for reversible logic circuits. A gate is reversible if the gate’s inputs and outputs have a one-to-one correspondence, i.e. there is a distinct output assignment for each distinct input combination. Therefore, a reversible gate’s inputs can be uniquely determined from its outputs. Reversible logic gates must have an equal number of inputs and outputs. Then the output rows of the truth table of a reversible gate can be obtained by permutation of the input rows. Reversible logic circuits have been emerged as a promising technology in the field of information processing, for example, majority data processing to preserve intelligence or medical signal to prevent data loss or revert back data modification. Irreversible computation results in energy dissipation due to data loss [10]. On the other hand, the reversible logic circuits offer an alternative form that allows computation with arbitrary small energy dissipation [11].

2. OPERATIONAL PRINCIPLE OF TOAD BASED OPTICAL SWITCH
TOAD based gate has taken an important role in optical communication and information processing [12-24]. Sokoloff et al. [17] demonstrated a TOAD capable of demultiplexing data at 50 Gb/s.

The TOAD consists of a loop mirror with an additional intraloop 2x2 (ideally 50:50) coupler. The loop contains a control pulse (CP) and a nonlinear element (NLE) that is offset from the loop’s midpoint by a distance \( \Delta x \) as shown in Fig. 1.

A signal with field \( E_{in}(t) \) at angular frequency \( \omega \) is split in coupler. It travels in clockwise (cw) and counter clockwise (ccw) direction through the loop. The electrical field at port-1 and port-2, can be expressed as follows.

\[
E_{out,1}(t) = E_{in}(t-t_d)e^{-j\omega t_d}
\left[d^2\cdot g_{ccw}(t-t_d) - k^2\cdot g_{cw}(t-t_d)\right]
\]

(1)

\[
E_{out,2}(t) = jdkE_{in}(t-t_d)e^{j\omega t_d}
\left[g_{cw}(t-t_d) + g_{ccw}(t-t_d)\right]
\]

(2)

Where \( I_d \) is pulse round trip time within the loop as shown in the Fig. 1. Coupling ratios \( k \) and \( d \) indicate the cross and through coupling, respectively. The cw signal be amplified by the complex field gain, \( g_{cw}(t) \), while ccw by \( g_{ccw}(t) \). The output power at port-1 can be expressed as,

\[
P_{out}(t) = \frac{P_{in}(t-t_d)}{4}\left|G_{in}(t) + G_{out}(t) - 2\sqrt{G_{in}(t)G_{out}(t)}\cos(\Delta \phi)\right|
\]

(3)

where, \( SW(t) \) is the transfer function. The phase difference between cw and ccw pulse is defined by \( \Delta \phi = (\phi_{cw} - \phi_{ccw}) \). The symbols \( G_{in}(t), G_{out}(t) \) indicate...
the respective power gains. Power gain is related with the field gain as 
\[ G = g^2 \quad \text{and} \quad \Delta \varphi = -\frac{\alpha}{2} \ln \left( \frac{G_{cw}}{G_{ccw}} \right). \]

Now we will calculate the power at port-2
\[ P_{out,2}(t) = \frac{1}{2} E_{out,2}^*(t) \cdot E_{out,2}(t) \]
\[ = -d^2 k^2 \cdot P_n(t-t_d) \cdot g_{ccw}^2(t-t_d) \]
\[ \cdot \left\{ 1 + \frac{g_{cw}^2(t-t_d) + \cos[\varphi_c(t-t_d) - \varphi_{cw}(t-t_d)]}{g_{cw}^2(t-t_d)} \right\} \]
\[ = \frac{1}{2} d^2 k^2 \cdot P_n(t-t_d) \cdot g_{cw} \left[ 1 + \frac{G_{cw}}{G_{cw}} + 2 \frac{G_{ccw}}{G_{cw}} \cos[\Delta \varphi] \right] \]
\[ = \frac{1}{2} d^2 k^2 \cdot P_n(t-t_d) \cdot \left\{ G_{cw} + G_{ccw} + 2 \sqrt{G_{cw} \cdot G_{ccw}} \cos[\Delta \varphi] \right\} \quad (4) \]

For ideal 50:50 coupler, \( d^2 = k^2 = \frac{1}{2} \). In the absence of a control signal, data signal (incoming signal) enters the fiber loop, pass through the SOA at different times as they counter-propagate around the loop, and experience the same unsaturated amplifier gain \( G_0 \), recombine at the input coupler i.e. \( G_{cw} = G_{cw} \). This leads to \( \Delta \varphi = 0 \). So expression for \( P_{out,1}(t) = 0 \) and \( P_{out,2}(t) = G_0 \cdot P_n \). It shows that data is reflected back toward the source. When a control pulse is injected into the loop, it saturates the SOA and changes its index of refraction. As a result, the two counter-propagated data signals will experience a differential gain saturation profiles i.e. \( G_{cw} \neq G_{cw} \). Therefore, when they recombine at the input coupler, the data will exit from the output port-1. For this case, the mathematical forms of two output powers can be expressed as, \( P_{out,1}(t) = \frac{P_{in}(t-t_d)}{4} \cdot SW(t) \) and \( P_{out,2}(t) \approx 0 \). Result of numerical simulation with Matlab7.0 has been shown in Fig. 2. In this simulation line-width enhancement factor of SOA (\( \alpha \)) was taken 9.5 and the ratio \( G_{cw} / G_{cw} \) was taken 0.52.

A polarization or wavelength filter may be used at the output to reject the control and pass the input pulse. Now it is clear that in the absence of control signal, the incoming pulse exits through input port of TOAD and reaches the output port-2 as shown in Fig. 2. In this case no light is present in the output port-1. But in the presence of control signal, the incoming signal exits through output port of TOAD and reaches the output port-1 as shown in Fig. 1. In this case no light is present in the output port-2.

In the absence of incoming signal, Port-1 and Port-2 receive no light signal as the filter blocks the control signal.
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as 2, since its optical implementation requires 2 TOAD-based switches. The delay of all optical TNOR gate is $1\Delta$, as in its optical design two TOAD switches works in parallel.

(a)

\[ P = A \]
\[ Q = B \]
\[ R = (A + B) \oplus C \]

(b)

**TABLE II**

<table>
<thead>
<tr>
<th>Inputs</th>
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<tbody>
<tr>
<td>A</td>
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4. SIMULATION AND RESULT

Simulation is done with Matlab-7. Figure 7(a), (b) and (c) are the three inputs A, B and C respectively. And figure 7(d) to (j) are the simulation results of figure 6(a) to 6(g) respectively.

5. PROPOSED ALL OPTICAL PNOR GATE

This proposed all optical PNOR gate is a (3x3) conservative optical reversible gate with the inputs to outputs mapping as \((A, B, C)\) to \((P = A, Q = A \oplus B, R = (A + B) \oplus C)\), where A, B, C are the inputs and P, Q, R are the outputs, respectively. The proposed all optical PNOR gate can be used as the replacement of existing NAND based all optical Peres gate [26].

The truth table of all optical PNOR gate is given in Table 3. An all optical PNOR gate can be implemented using 4 TOAD-based switches, 7 beam splitters (BS) and 3 beam combiners (BC). Figure 5(a) and Fig. 5(b) show the all optical implementation of PNOR gate and the block diagram, respectively.

The optical cost of PNOR gate is considered as 4 as its optical implementation requires 4 TOAD-based switches. The all optical PNOR gate has delay of $1\Delta$ as in its optical design four TOAD switches works in parallel.
6. SIMULATION AND RESULT
Simulation is done with Matlab-7. Figure 7(a), (b) and (c) are the three inputs A, B and C respectively. And figure 7(d) to (j) are the simulation results of figure 6(a) to 6(g) respectively.

7. APPLICATION OF TNOR GATE AS UNIVERSAL GATE
TNOR gate can be used to perform as universal logic gate. Proposed arrangements to perform various gate operations are as follow.
8. SIMULATION AND RESULT

Figure 9(a), (b) and (c) are the three inputs A, B and C respectively. And figure 9(d) to (j) are the simulation results of figure 8(a) to 8(g) respectively. Simulation is done with Matlab-7.

![Simulation Results](image)

The vertical axis in all figures of simulation results indicates in dB, while horizontal axis represents time scale in ps.

9. CONCLUSION

In this paper, we have designed two new all optical reversible NOR gates for NOR based implementation of reversible boolean functions and arithmetic operations. The first all optical TNOR gate can be used as a replacement for existing all optical Toffoli gate, while the second all optical PNOR gate can be used as a replacement of all optical Peres gate. It is reported that the proposed all optical reversible NOR gates have significant advantages over existing reversible NAND gates in terms of optical cost and delay. So, these new optical reversible NOR gates can be profitable for minimizing the optical cost and delay of the optical reversible circuits. All the optical reversible gates are functionally verified at the logic level using Matlab-7. In conclusion, this paper helps the state of the art of reversible optical circuits by using the NOR logic based reversible gates as an alternative to NAND logic based reversible gates. The theoretical models developed and the results obtained numerically are useful to future all-optical reversible logic computing system.

10.REFERENCE


