Realization of a Low Power High Performance IC Design Technique for Wireless Portable Communication Devices used in Underground Mines

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ABSTRACT
The demand for increasing speed and low power dissipation triggers numerous research efforts with the increasing demand of wireless portable communication systems in underground mines driven by batteries. Presence of highly flammable gases in underground mines prohibits the use of higher power dissipating electronic systems. Low power wireless portable communication devices can safeguard the life of miners in case of disaster. The demand for increased battery life of portable devices has forced researchers to seek out new integrated circuit techniques to reduce the power dissipation without comprise in performance of the portable electronic system. Power consumption by the electronic system determines the battery life of the device. As a result, tremendous effort has been devoted to achieve lower power dissipation without affecting performance of portable communication devices. Therefore, reduction of power dissipation without sacrifice in performance is vital for wireless portable communication devices for improving the safety standards and productivity in underground mines. Multi threshold circuit technique can be used to design a low power high performance integrated circuit for wireless portable communication devices used in underground mines.

Keywords
Power dissipation, Portable device, Multi threshold circuit technique, Leakage current.

1. INTRODUCTION
Modern electronics and Information Technology, applied in the field of underground environmental conditions, play a significant role for enhancing underground mine safety and productivity[1]. Most of the existing communication systems present in underground mines are wired based. These communication systems are difficult to assemble in inaccessible places and are also prone to fail in case of disasters. Therefore, wireless portable communication system is convenient in day-to-day normal duty and even in disaster situations in underground mines. Minerals are extracted from underground mines, several hundred meters below the surface of the earth. Safety of miners working in underground mines is of great concern. Fig. 1[2] shows the entrance path of an underground mine and Fig. 2[2] shows disasters in underground mine due to roof collapse. The underground mining environment is hazardous and prone to several disasters including fire, roof collapse and highly flammable and poisonous gas leakage. The growing demand of portable communication devices with reduced power and reduced size in underground mines has opened a vast opportunity for the design of low power and compact Integrated circuit. According to Moore's law, the number of transistor quadruples every two to three years. Demands for low voltage and low power integrated circuits in portable devices have increased dramatically in recent days because of limited battery life. Multi-million transistor chips operating at hundreds of megahertz speed are already in use in portable communication devices[3].

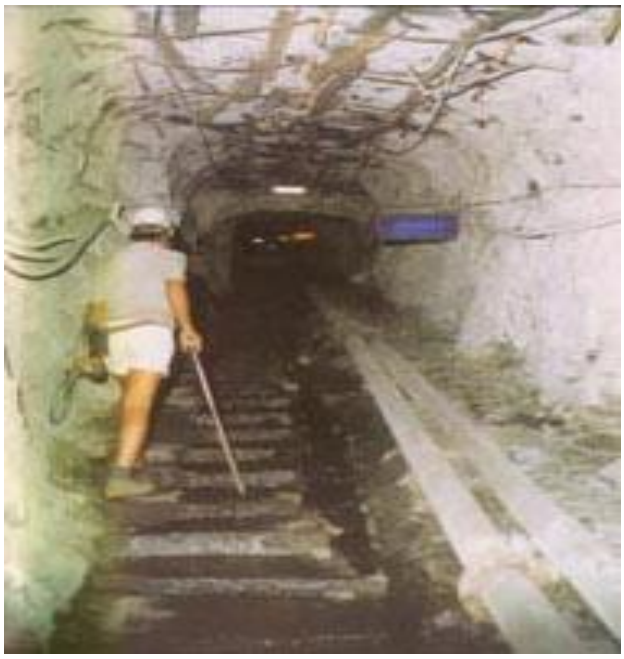

Fig1. Entrance inside an underground mine

The computational functionality and switching frequencies of electronic chips are increasing every year. High speed and high integration density chips have experienced an alarming rise of heat dissipation. With clock speeds exceeding 4 GHz and switching millions of transistors, chip temperature has reached to such a high level that requires expensive packaging and heat dissipation techniques. Fred Pollack of Intel made observations that power density is increasing at an increasing rate, approaching that of the hottest man-made objects on the planet, and graphed power density as shown in Fig.3[3]. Serious reliability issues arise when working at such high temperatures *[4]*

Fig 2. Disaster in an underground mine

A limited amount of energy stored in a small battery in portable devices requires extensive power management techniques to increase the battery life. The energy density given by new battery technologies is still low in view of increasing applications of portable devices. Therefore, reducing the power dissipation of integrated circuits without compromise in performance through new circuit design technique is a major challenge in portable Communication system design [5].

2. POWER DISSIPATION IN INTEGRATED CIRCUITS

Power dissipation in Integrated circuits can be divided into four categories: short-circuit power, switching power, leakage power and static power dissipations. Short-circuit power dissipation occurs when a conducting path between the supply voltage and the ground is formed. This component of power consumption is significant in dynamic circuits. Careful design is required to keep this component of power dissipation as small as possible. Switching power dissipation is a result of the power consumed in charging and discharging internal capacitances in the circuit. Leakage power dissipation occurs when the device is turned off. Leakage power forms a significant portion of the total power consumption as a result of the low threshold voltage devices. Static power consumption arises when the system or chip includes circuits other than conventional CMOS gates that have continuous current paths between the power supply and the ground.

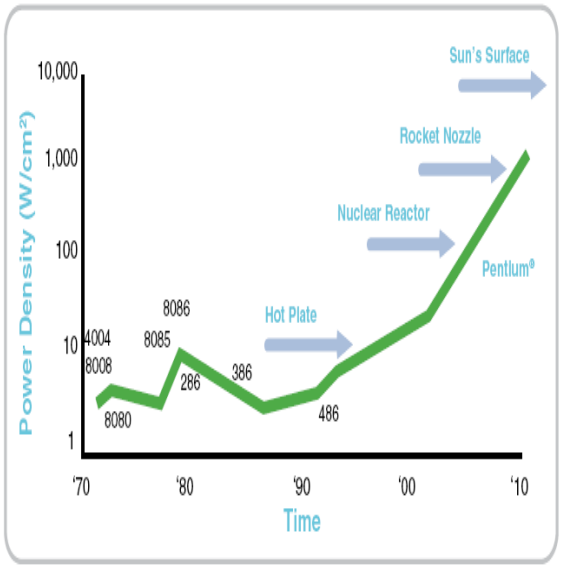

Fig. 3 Power density trends

3. LOW POWER DESIGN BY VOLTAGE SCALING

Several methods for power and energy reduction have been proposed [6]. Voltage supply scaling is considered as one of the most effective elements in the process of reducing power dissipation in integrated circuits [7]. Lowering the power supply voltage reduces the operational speed of the device. The operational speed of the device can be increased if the threshold voltage of the transistors, V_t is scaled down accordingly. However, this approach is limited because the threshold voltage may not be scaled down to the same extent as the supply voltage. When scaled linearly, reduced threshold voltages allow the circuit to produce the same speed performance at a lower supply voltage. Reducing the threshold voltage of transistor can improve its switching speed performance. However reducing the threshold voltage can also raise concern over noise margins and sub threshold conduction. Smaller threshold voltages of the device lead to smaller noise margins in the Integrated circuit. The subthreshold conduction current also sets a major limitation against reducing the threshold voltage. Leakage power is forming an increasing portion of the total power dissipated in modern technologies using low threshold voltage devices. Several techniques have been developed to reduce its impact. Thus, the relationship between power consumption and operation speed is critical in obtaining optimal scaled devices.

4. LOW POWER HIGH PERFORMANCE CIRCUIT DESIGN TECHNIQUE

Low threshold devices have caused a dramatic increase in the leakage current. Leakage power dissipation is associated with the low threshold voltage of the device. A direct and effective solution is to use low threshold voltage devices in the critical path and high threshold devices elsewhere. Multi Threshold technique can be used to design low power high performance integrated circuit for a wireless portable communication devices in underground mines.

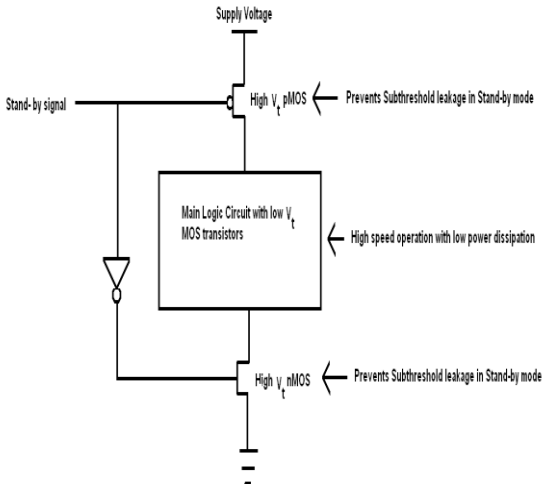

Fig.4. A logic circuit using multi threshold circuit technique

4.1 Multi Threshold Circuit Technique

The leakage current can be reduced by using multi threshold technique. In this technique, low threshold voltage device is used where faster evaluation is needed while a high threshold voltage device is used to disconnect the main circuit from the power supply during stand-by mode. Fig. 4[8] shows representation of a logic circuit using multi threshold circuit technique. Low threshold MOS transistors are typically used to design the main logic circuit where switching speed is essential, whereas high threshold transistors are used to effectively isolate the main logic circuit from the power supply and the ground in stand-by mode. In active mode of operation, the high threshold transistors are turned on and the main logic circuit consisting of low threshold voltage transistors can operate with low leakage power dissipation and high switching speed. When the circuit is driven into stand-by mode, the high threshold transistors are turned off and the conduction path for any sub threshold leakage current that may originate from the main logic circuit is effectively cut off.

5. CONCLUSION

Low power high speed integrated circuit design has become a necessity especially for wireless portable communication devices in underground mines. Power dissipation causes a real threat for the reliability of the portable device with increase in the integration of electronic components. As a result, tremendous effort has been devoted to achieve lower power dissipation without sacrifice in performance of the device. Many techniques have been introduced to control this increasing power dissipation component on all levels of design abstraction. System, circuit and device levels are examined for potential solutions for overall power reduction. The dramatic increase in transistor densities in modern integrated chips has lead to tremendous increase in power dissipation. This trend will continue to grow as more transistors are packed into the same area in order to reduce the size of the device. In order to overcome these difficulties, multi threshold technique can be used to design a low power high performance integrated Circuit for wireless portable communication devices used in underground mines for better productivity and safety of miners.

6. REFERENCES

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