TCAD Simulation of Tunnel Field Effect Transistor

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ABSTRACT
It is observed that there are two limitations with conventional MOSFET, especially Sub threshold swings and high Ioff current. Subthreshold has minimum value of 60 mV/decade [1]. But we cannot get lower sub-threshold swing than this value with conventional MOSFET. These limitations are overcome by Tunnel Field effect transistors (TFET). TFET is working on tunneling effect, which requires less input voltages to decrease band gap due to presence of p-i-n region. Also there are very low OFF- current in TFET and hence low power consumption. The TFET works on band-to-band tunneling (BTBT) principle. In this paper, principle operation of TFET has been studied, and then simulation of the TFET using Sentaurus TCAD software.

Keywords
Band to band tunneling, TFET, tunnel field effect transistor, low voltage operating transistor.

1. INTRODUCTION
It has been studied that in the integrated circuit fabrication, MOSFET technology has been used. It has been studied; the integrated circuit fabrication is done according to a law popularly known as Moore's law [2]. To fulfill this law, it is required to do the scaling of MOSFET, because of scaling in MOSFET some issues has been raised like short channel effect, drain induced barrier lowering, punch through effect, tunneling effect, velocity saturation, velocity overshoot, large process parameter variations and higher leakage current[2]-[7]. To avoid these issues several technologies have been introduced like double gate MOSFET, Finfet technology, gate all around and TFET (tunnel field effect transistor) etc. Among these technologies TFET is the most appropriate technology for the fabrication of integrated circuits, because it has lower subthreshold swing than 60mV/decade, lower off-current and lower power dissipation.

2. DEVICE OVERVIEW
TFET (tunnel field effect transistor) is commonly referred as gated p-n diode with an intrinsic channel as shown in figure 1. In order to make it similar with MOSFET the name of the node or terminal are given same as MOSFET i.e. gate, source and drain. The terminal voltages are named as gate voltage (V_g), source voltage (V_s) and drain voltage (V_d) [8]. The difference between MOSFET and TFET physically is that, in TFET both the dopant are different one is of p-type and one is of n-type where as in MOSFET both the dopant are of same type either of p-type or n-type. TFET works in both modes i.e. in p-mode (PTFET) and in n-mode (NTFET). When the gate voltage is less than zero and drain voltage is negative then it is working in p-mode and known as PTFET. Likewise when the gate voltage is greater than zero and drain voltage is positive then it is working in n-mode and known as NTFET. The current conduction in TFET is due to band- to-band tunneling phenomenon [9].

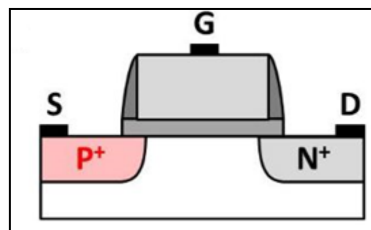

Figure 1 TFET (tunnel field effect transistor)

3. BASIC THEORY OF TFET OPERATIONS
The basic theory of TFET operation can be understood easily with the help of band diagram. It has been studied that current flow in the TFET is because of band to band tunneling. In band-to-band tunneling the electron is moved from the valence band of one semiconductor to the conduction band of the other semiconductor. To understand the tunneling phenomenon in TFET let us consider a NTFET as shown below [10].

Case 1: When (Vd = Vg = Vs = 0 V) called relaxed state then no current is flowing there, shown in figure 2[10].

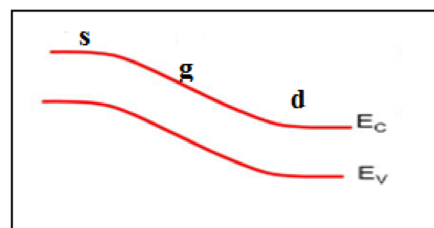

Figure 2 Energy band diagram of TFET at zero bias

Case 2: Vg set to its nominal positive value and Vd low, and then the tunneling occurs at the source /channel interface, shown in figure 3[10].

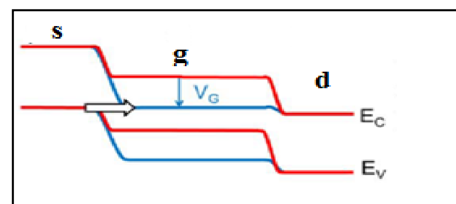

Figure 3 Energy band diagram of TFET when gate voltage

Case 3: Vg nominal and Vd increased, tunneling now occurs in both junctions at equal rate, shown in figure 4[10].

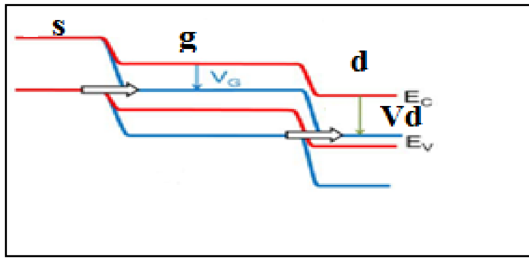

Figure 4 Energy band diagram when Vg is nominal and Vd is increased

Case 4: Vg nominal and Vd very high: the tunneling at the source/channel junction is still present, but negligible compared with the tunneling at the channel/drain junction, shown in figure 5[10].

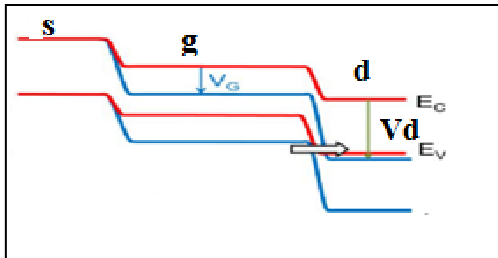

Figure 5 Energy band diagram when Vg is nominal and Vd is very high

4. FABRICATION STEPS OF TFET USING PROCESS SIMULATION OF SENTAURUS TCAD

In this paper, fabrication of tunnel field effect transistor (TFET) is done by process simulation in Sentaurus TCAD tool.

In the fabrication process, in first step SOI substrate is prepared. In the next step, mesa isolation is done to electrically isolate the transistor, as shown in figure7 (a). Then the gate oxidation is done at 900 °C temperature. After that poly-si deposition is done by using LPCVD (low pressure chemical vapor deposition) process. In the next step SiO2 deposition is done by LPCVD process. This deposited layer of SiO2 act as hard mask for etching process. Then poly-si activation is done at 900 °C temperature for 1 min, as shown in figure7(b). After that gate patterning is done through lithography, as shown in figure7(c). Then source and drain implantation is done, as shown in figure7 (d). To prevent from the lattice damage during the implantation annealing is carried out at 950 °C temperature in pure N2. Oxide isolation is done to prevent from surface leakage and surrounding air and then vias are opened by optical lithography, as shown in figure7 (e). In the next step metallization is done and then post metal annealing is done to improve the metal/silicon interface at 450 °C temperature for 15 min, as shown in figure7(f).

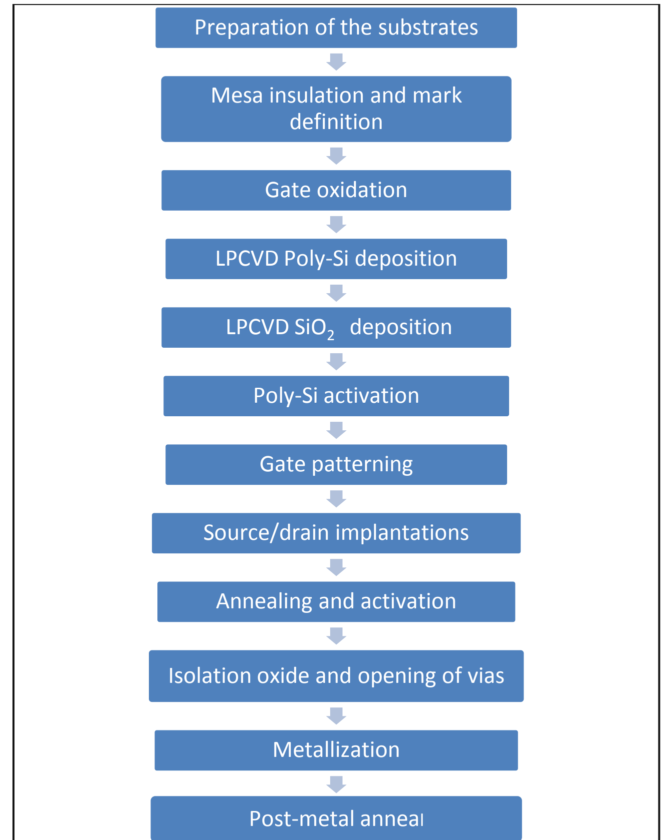

Figure 6 Fabrication steps of TFET

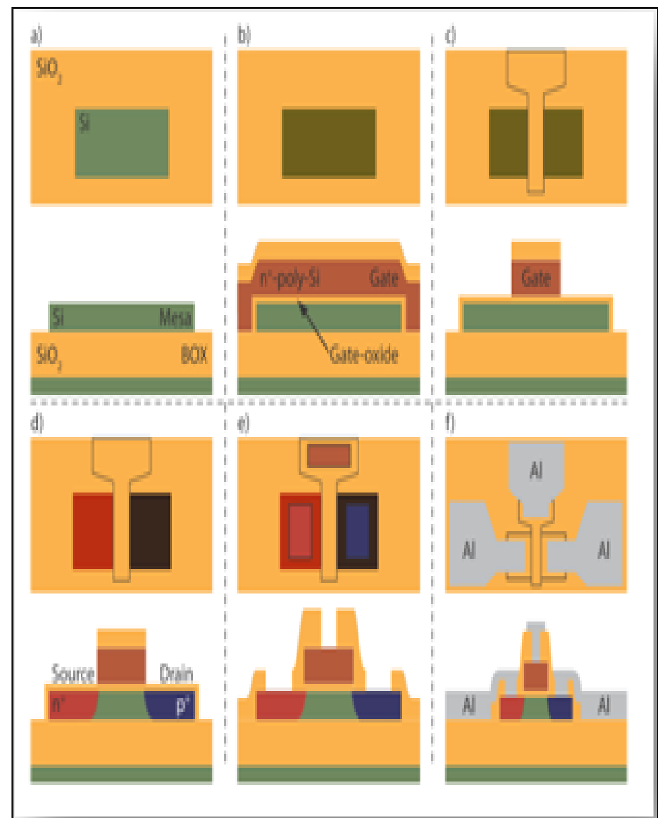

Fig 7 Diagrammatic representation of fabrication steps of TFET

5. SIMULATION RESULTS

Using process simulation of Sentaurus TCAD, device structure is analyzed and its insight operations are also analyzed which includes acceptor concentration, donor concentration, band gap narrowing, and characteristics of drain current with respect to drain to source voltage.

In figure 8, TFET structure designed in TCAD tool, represents the drain and source region, mesa isolation, poly-Si deposited layer of the TFET.

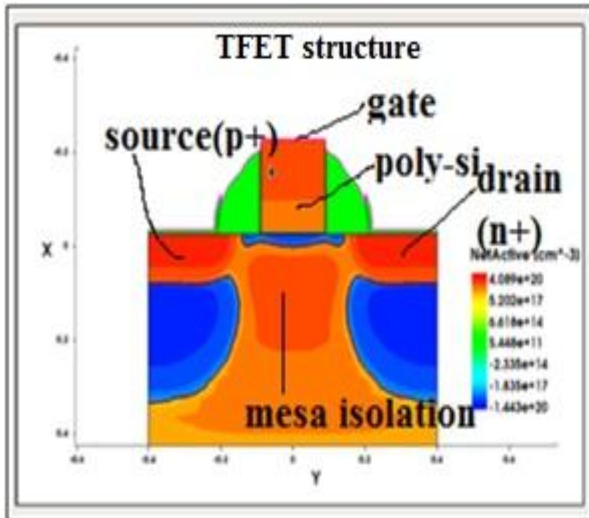

Fig 8 Simulated structure of TFET in TCAD

Mesa isolation is done to electrically isolate the transistor and to protect the high power devices. Here, poly-Si layer is used as a conducting material for gate. Source and drain are the dopant regimes of the TFET. The color bar on the right side of the figure 8 shows the concentration of different materials used in fabrication.

Figure 9 represents the acceptor concentration. The level of acceptor concentration has been analyzed by matching the color with the side color bar. It shows that at dopant region and on the top of channel region have maximum acceptor concentration i.e.3.921e+20 cm^{-3}.

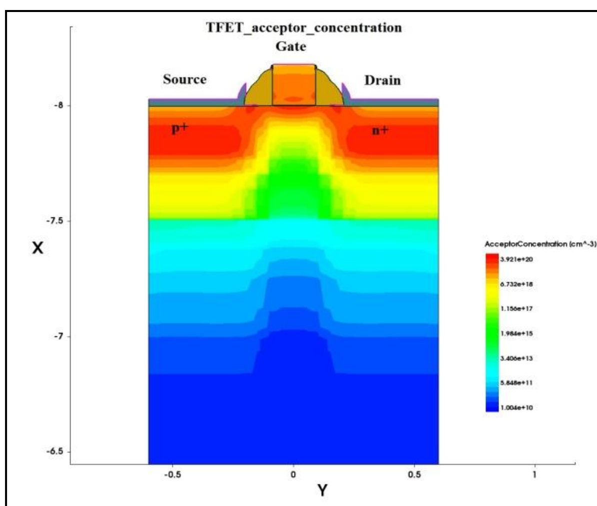

Fig 9 Acceptor concentration

Figure 10 represents the donor concentration. The donor concentration is highest in the source and drain region (red) i.e. 1.686e+21 cm^{-3} and lowest in middle which is showed with blue color i.e.1.015e+10 cm^{-3}.

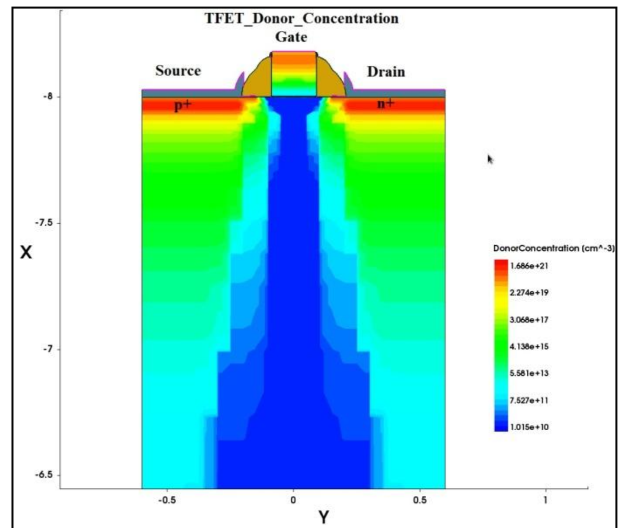

Fig 10 Donor concentration

Figure 11 represents the band gap narrowing. The band gap narrowing is highest in the top regime of source and drain region (red) i.e. 1.765e-01eV and lowest in substrate region (blue) i.e. 0.0eV.

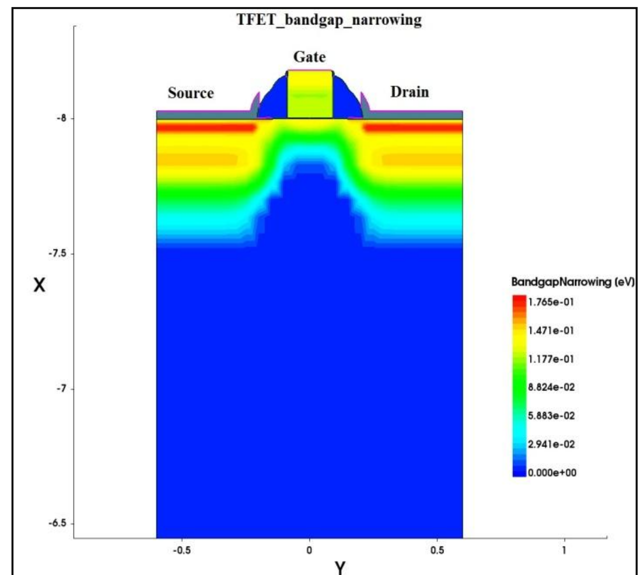

Fig 11 Band gap narrowing

Figure 12, represents the characteristics of drain current with respect to drain to source voltage. It shows that drain current is linearly increased with the increase in the drain to source voltage up to pinch off point. The value of drain current obtained is 0.001A.

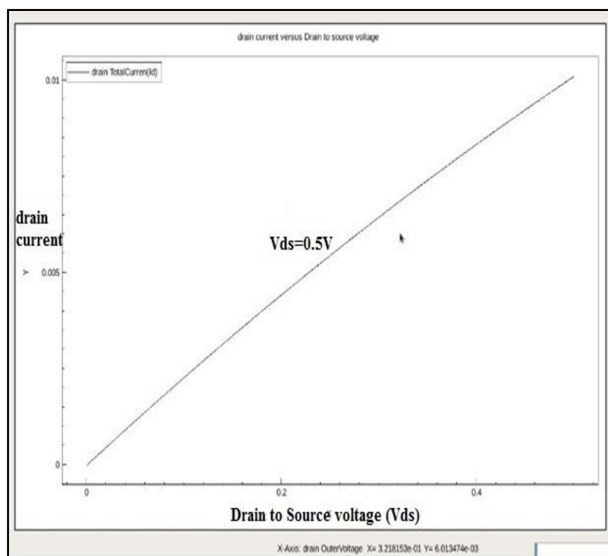

Fig 12 Characteristics of drain current with respect to drain to source voltage

Table 1. Obtained Results after simulation

Parameters	Values
Acceptor Concentration	3.921e+20 cm^{-3}
Donor concentration	1.686e+21 cm^{-3}
Band gap Narrowing	1.765e-01eV
Drain current	0.001 A

6. CONCLUSION AND FUTURE

In this paper, inner operation of TFET has been studied. The conduction mechanism in TFET is band to band tunneling. It has lower subthreshold swing because of which it works as a faster switch than the conventional MOSFET. Also it has lower off current and power consumption that is why it is also known as green transistor. The simulation result demonstrates the drain current of 0.001A in the device at V_{DS} =0.5V. While the acceptor concentration in the device is 3.921e+20 cm^{-3}, donor concentration is 1.686e+21 cm^{-3} and band gap narrowing observed is 1.765e-01eV.

In future, for the improvement of TFET performance different structured TFETs can be fabricated like double gate TFET, junction less TFET, doping less TFET etc. and based on the simulated results the device finds a good role in modern analog applications.

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