UART Designing for Four Different Baud Rate for Cyclone III Family

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ABSTRACT
UART (Universal Asynchronous Receiver Transmitter) is used for short-distance, low speed, low-cost data exchange between computer and peripheral. They provide a means to send data with a minimum of wires. The data is sent bit-serially, and no clock signal is sent along with it. The fact that a clock is not transmitted with the data complicates the design of a UART. The two systems (sender and receiver) have separate, unsynchronized, clock signals. The programmable logic devices can be used for such application by developing core for UART. By using hardware descriptive language UART simulation can be tested before it can be loaded on programmable device. In this project we present UART which includes three modules which are the baud rate generator, receiver and transmitter.

Keywords
UART, Cyclone III,VHDL,Four baud rates

1. INTRODUCTION
Asynchronous serial communication has advantages of less transmission line, high reliability, and long transmission distance, therefore is widely used in data exchange between computer and peripherals. UARTs are used for communication between two devices. They provide a means to send data with a minimum number of wires [5]. The data is sent bit-serially, and no clock signal is sent along with it. The primary function of a UART is parallel- to-serial conversion when transmitting, and serial-to-parallel conversion when receiving. The fact that a clock is not transmitted with the data complicates the design of a UART. The two systems (sender and receiver) have separate, unsynchronized, clock signals. Although the two clocks will have the same frequency, they will not have the same phase. Part of a UART's function, and the tricky part, is to "sample" the serial input at just the right time to reliably capture the bit stream. A high-speed clock to sample the bit stream multiple times per data bit allows one to accomplish this task.
In this project, we focused on designing the UART (Universal Asynchronous Receiver Transmitter) for four different types of baud rate; using computer simulation (VHDL).Here we are working on cyclone III family and device name is EP3C55F484C8.

2. BLOCK DIAGRAM OF UART

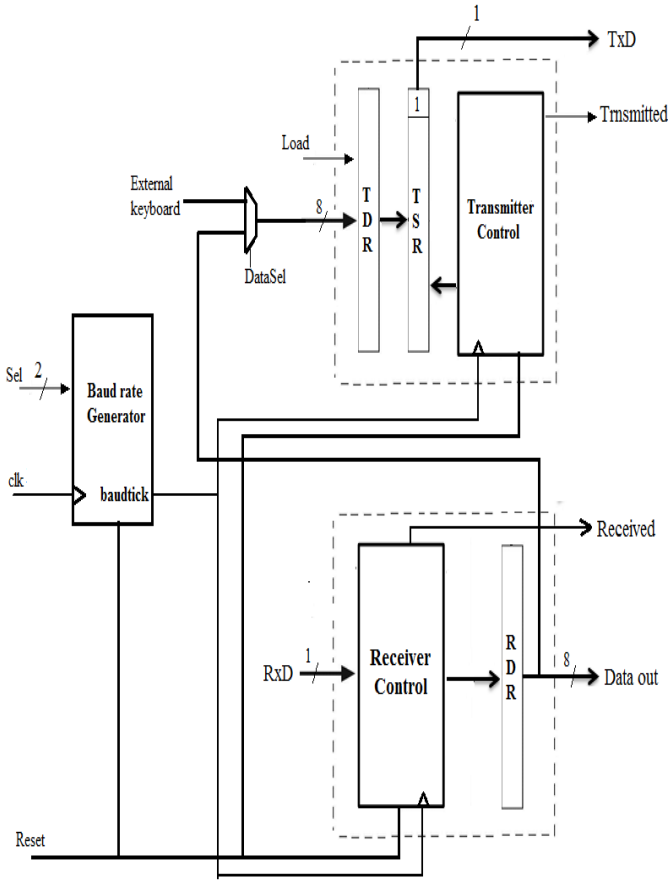


Fig.1 Block Diagram of UART

UART Components
A UART is composed of three main component receiver, transmitter and baud rate generator.

Inputs:
Sel: Selects baud rate (4 options are available).
RxD: Data coming from PC serial port.
DataSel: Selects whether data to be transmitted is coming from external keyboard attached to FPGA or data coming from pc serial port.
Reset: Resets all components.

Outputs:
TxD: Data is sent to pc serial port and displayed.
Data Out: Data received is shown on LED's on FPGA. In case parity check fails, then output is always shown as "E".

3. BAUD RATE GENERATOR

The baud rate generator generates a sampling signal whose frequency is exactly 16 times UART's baud rate. If the baud rate is X, the sampling rate has to be 16*X ticks per second. The system clock rate is 50 MHz the baud generator needs a mod-m ($50*10^6/16*X$) counter, in which 1 clock-cycle-tick asserted once every m clock cycle [6].
The baud generator has 2-select bit to decide baud rate, since we are using two bits, we have the choice of four baud rates.

Table 1. Baud Selection

Bit Select	BAUD Rate
00	9600
01	4800
10	38400
11	19200

4. TRANSMITTER

Transmitter takes parallel data and sends it serially on the TxD pin. The transmitter consists of TDR (Transmit Data Register), TSR (Transmit Shift Register) and controller. As load signal goes high transmitter transfers data from TDR to TSR and outputs start bit "0" to the TxD pin then shifts TSR right eight times to transmit 8 bits. When eight data bits transmitted ,transmitter sends parity bit and finally outputs stop bit"1" to the TxD pin and signal "transmitted" goes high.

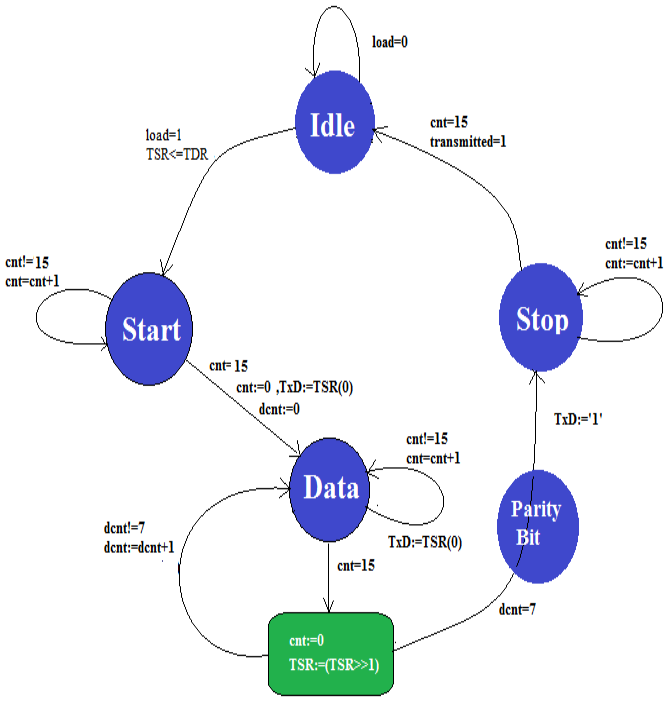


Fig.2 State Diagram of Transmitter

5. RECEIVER

Receiver takes data serially in RxD pin, and provides the parallel to the Data out pin. UART receiver consists of RDR (Received Data Register) and controller. When the UART detects start bit receiver reads and shifts 8 data bits serially into a temporary register. When 8 data bits has been received and parity check passes then after stop bit has been received controller transfers data from temporary register to RDR and received signal goes high. If parity check fails then, output of receiver is always shown as "E".

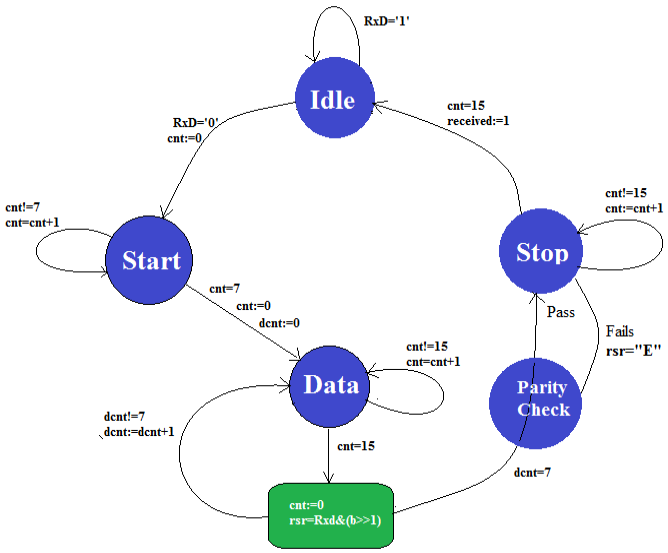
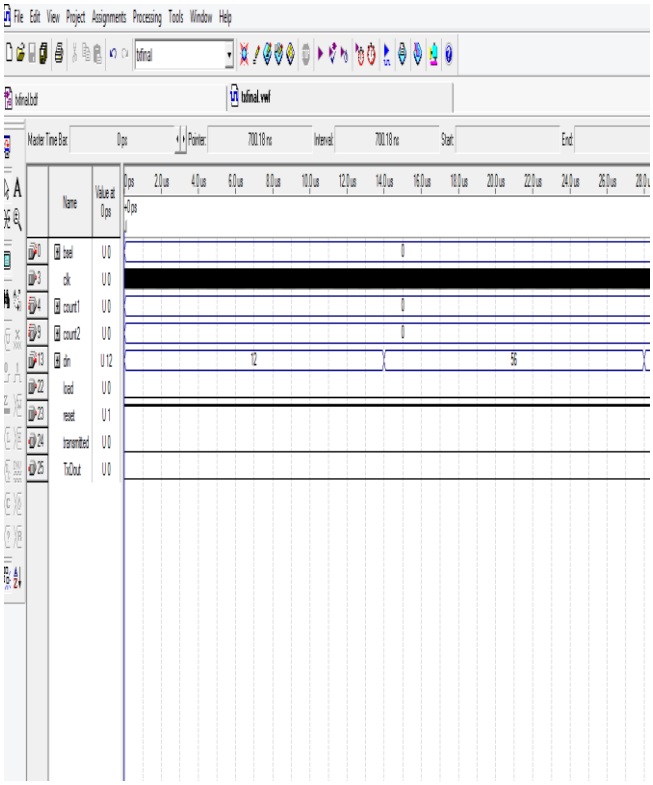


Fig.3 State Diagram of Receiver

6. SIMULATION RESULTS

(Transmitter & receiver block)

Transmitter



RECEIVER

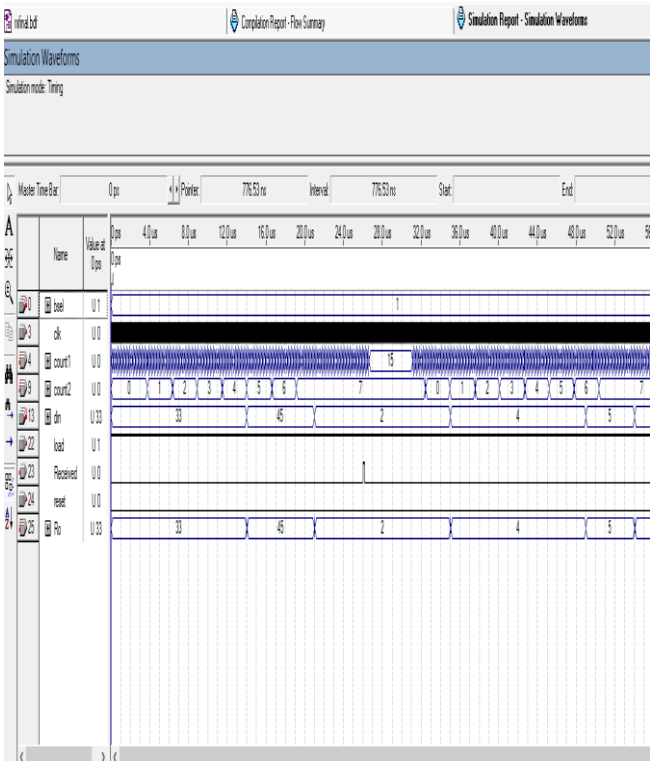
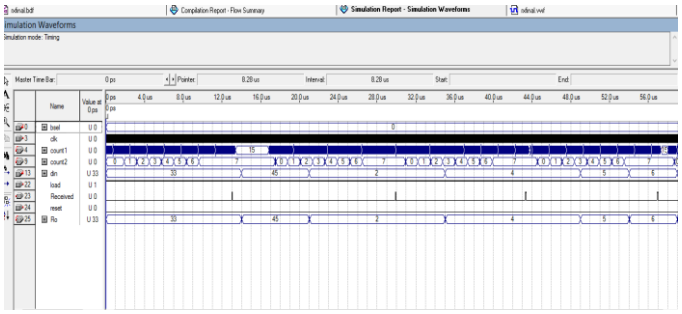


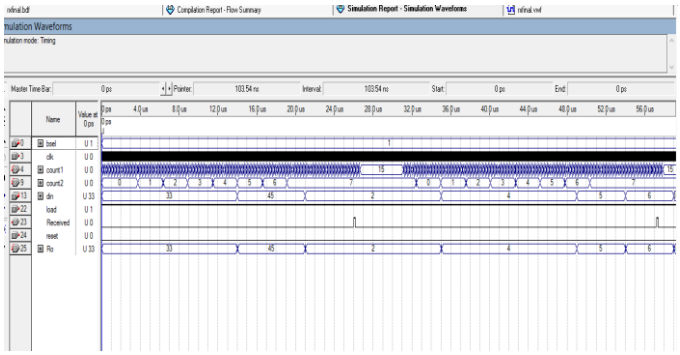
Fig.4 Simulation result of transmitter and receiver

7. SIMULATION RESULTS OF FOUR DIFFERENT BAUD RATE

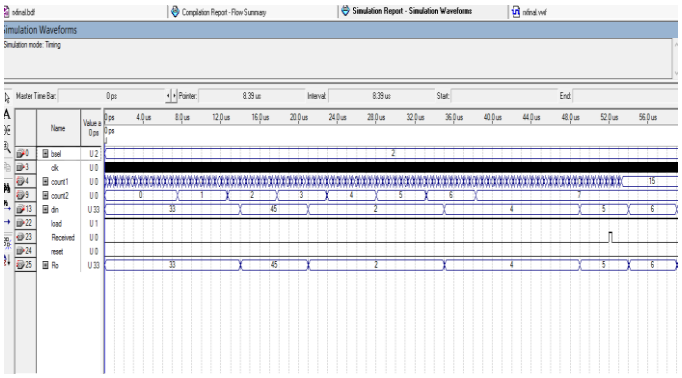
I. Bit select=00



II. Bit select=01



III. Bit select=10



IV. Bit select=11

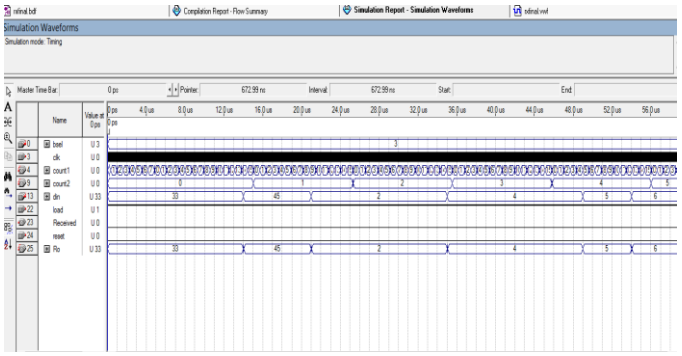


Fig.5 Simulation results of four different baud rates

8. CONCLUSION

Here VHDL language is used to get the modules of UART.

These results are the outcome of cyclone III (EP3C55F484C8) family. UART for four different types of baud rate; using computer simulation (VHDL) is successfully designed.

9. REFERENCES

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