Channelization and Frequency Tuning using FPGA for UMTS Baseband Application

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ABSTRACT

Wireless base station transceiver front- end signal processing often is performed using digital techniques. As bandwidths and IF digital-analog sampling frequencies increase, a large number of calculations are required for channelization, frequency tuning, and rate conversion. As new standards emerge, the design options are numerous for multi-protocol and multichannel transceiver front ends. The inherent flexibility of Xilinx FPGAs along with recent advances in their architectures makes them ideal for cost-efficient implementations of digital transceiver front-end functions, such as down conversions and precise channel filtering. The Xilinx development environment for digital signal processing (DSP) functions provides all of the resources needed for simultaneously developing signal processing algorithm and circuit parameters. This paper describes a design using some IP cores of Xilinx system generator and simulink software in designing the single channel to multichannel digital down converters (DDCs) for UMTS base stations. The four- channel implementations are described that efficiently map the DSP algorithms into the resources of the Virtex®-5 families of FPGAs.

KEYWORDS

 IF, FPGA, DSP, DDC, CDMA, UMTS.

1. INTRODUCTION

The widespread use of digital representation of signals for transmission and storage has created challenges in the area of digital signal processing. The applications of digital finite impulse response (FIR) filter and up/down sampling techniques are found everywhere in modem electronic products where lower circuit complexity is always an important design target,since it reduces the cost. There are many applications where the sampling rate must be changed. Interpolators and decimators have been utilized to increase or decrease the sampling rate. Down sampler are used to change the sampling rate of digital signal in multi-rate DSP systems.

This rate conversion requirement leads to production of undesired signals associated with aliasing and imaging errors. So some kind of filter should be placed to attenuate these errors. Recently, there is increasingly strong interest on implementing multimode terminals, which are able to process different types of signals, E.g. WCDMA, GPRS, WLAN and Bluetooth.

2. DESCRIPTION OF DDC

The Digital down Converter (DDC) as shown Figure 1. a digital circuit which implements the conversion of a complex digital baseband signal to a real pass band signal. The input complex baseband signal is sampled at a relatively low sampling rate, typically the digital modulation symbol rate. The baseband signal is filtered and converted to a higher sampling rate before being modulated onto a direct digitally synthesized (DDS) carrier frequency. The DDC typically performs pulse shaping and modulation of an intermediate carrier frequency appropriate for driving a final analog up converter and is used extensively in wireless and wire line communication systems.
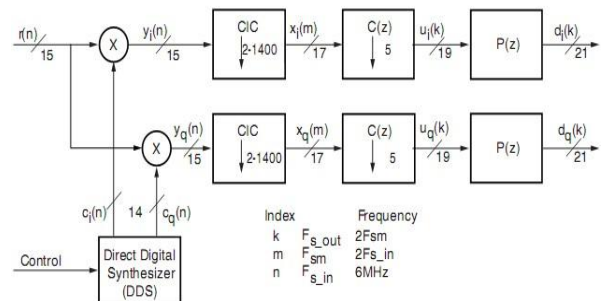

Figure 1: Digital down Converter Block diagram

3.MULTI-CHANNEL

These implementations are optimized to minimize the logic resources required within the low-cost Xilinx Virtex®-5 FPGAs. Optimal cost is achieved through time-sharing processing element resources that support multiple individual channels of data. Processing elements are tuned to use every clock cycle where possible, performing the maximum amount of computation per silicon resource the four channel *digital down conversion* as shown in figure 2.
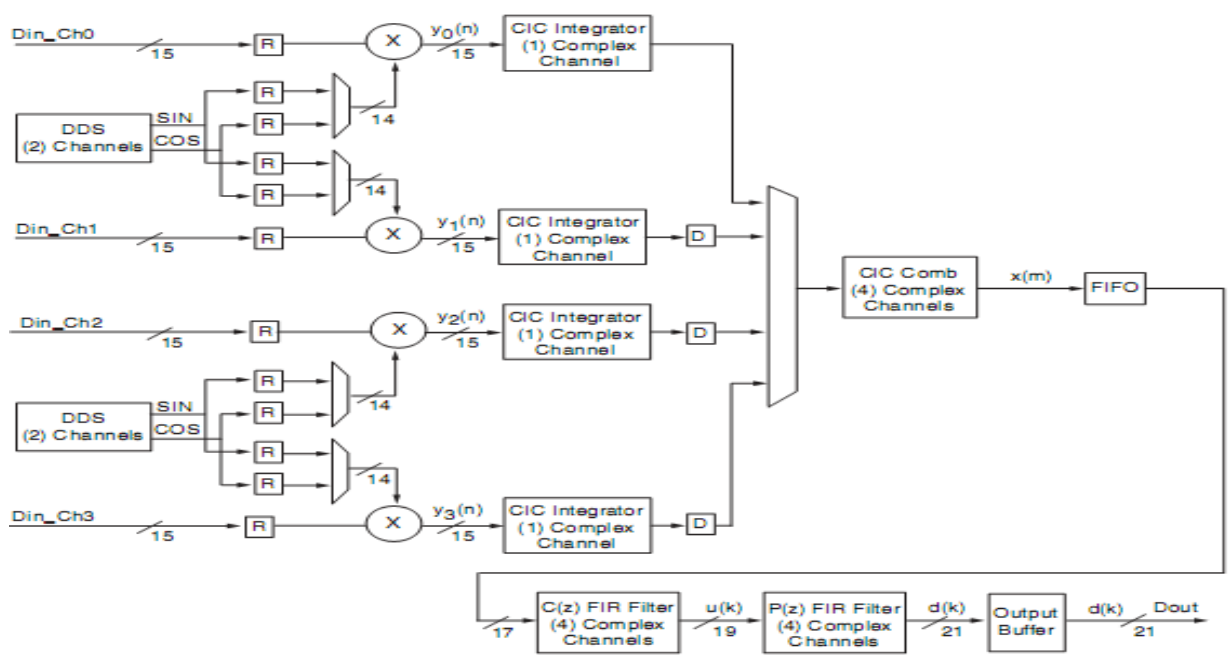
Figure 2: Four-Channel UMTS DDC Implementation

A) Filters

Two types of filters are required to implement the DUC solutions specified in this FIR and CIC. FIR filters typically are implemented in Xilinx FPGAs using either the MAC engine or the DA technique The DUC consists of following blocks Are MAC fir filter, Cascaded Integrator Comb (CIC) filter, Direct Digital Synthesizer (DDS) and Multiplier.

B) MAC-Based FIR Filter

The Xilinx MAC FIR core implements a highly configurable, high-performance, and area efficient FIR filter. Single-rate polyphase decimators and interpolators are supported. Multiple data channel operation is supported for all filter types. Symmetry in the coefficient set is exploited for single MAC implementations to increase overall performance and minimize resource utilization. All internal data-paths provide full-precision arithmetic to avoid the possibility of overflow. The full-precision sum-of-products is presented on the Data Output port. A set of three handshake control signals provides an easy-to-use user interface.

The MAC FIR core uses one or more time-shared multiply accumulate (MAC) functional units to service the N sum-of-product calculations in the filter. The core automatically determines the minimum number of MAC engines required to meet the user specified throughput. Figure 2 is a block diagram of a single MAC engine. The figure shows storage for the filter coefficients, sample store and the control circuit that sequences the appropriate coefficients and data to the multiply-accumulator for the specified integration period [7].

The MAC-based architecture uses a multiplier to perform the tap product calculations, followed by an accumulator to perform the filter addition operations. Figure 3 illustrates a single MAC engine FIR filter. When a filter operation rate exceeds that of a single MAC,

multiple MACs are placed in parallel, and the individual results are then added together to form the final filter result
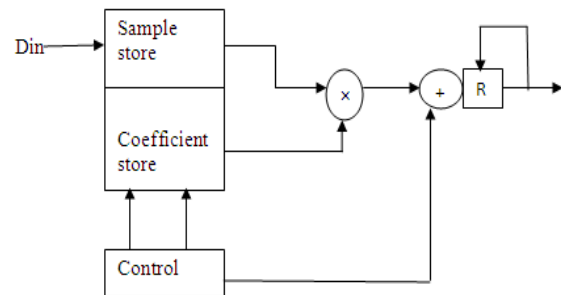

Figure 3: Multiplier-Accumulator FIR Filter

1). Multiple MAC Engine Filters

The MAC FIR core automatically generates an implementation that meets the user defined throughput requirements based on the system clock rate, sample rate, number taps and channels, and rate change. The core inserts one or more multipliers to meet the overall throughput requirements. The number of multipliers required for a filter is determined by computing the number of clocks available to process each input sample (A) and then dividing the number of multiplies required to perform the computation (B) by A. The number of clocks available to process each input sample is found by [7]:
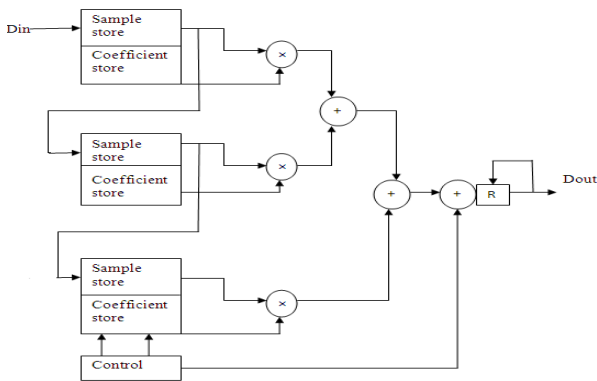
Figure 4: Three-MAC Engine FIR Filter.

C). Cascaded Integrator Comb (CIC) Filters

Cascaded integrator-comb, also called as Hogenauer filters, are multi-rate filters that are used for realizing large sample rate conversions in digital systems. The main advantage of this filter is it does not use multipliers, and consists of only adders, sub-tractors and registers. A CIC filter is typically used in applications where the system sample rate is much larger than the bandwidth occupied by the signal. They are commonly used to build Digital down Converters (DDCs). Some applications that uses the CIC filter include software designed radios, cable modems, satellite receivers, 3G base stations, and radar system.

1). CIC decimators [3].

Figure 5 shows the basic structure for a CIC decimation filter. The integrator section consists of N ideal integrator stages operating at the high sampling rate Fs. Each stage is implemented as a one-pole filter with a unity feedback coefficient. The transfer functions for a single integrator is the comb section operates at the low sampling rate fs / R where R is the integer rate change factor. This section consists of comb stages with a differential delay of M samples per stage. The differential delay is a filter design parameter used to control the filter"s frequency response. M is restricted to be either 1 or 2. The transfer function for a single comb stage, referenced to the high input sample rate
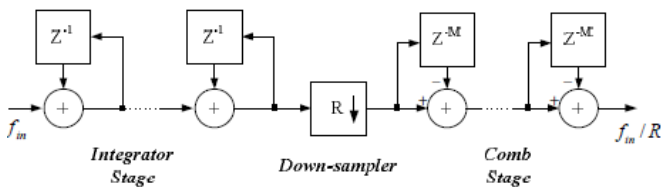

Figure 5: CIC decimator Structures [3].

The CIC decimator filter is composed of a series of N integrator section followed by a series of N comb section the differentiators run at the filter input signal sampling rate Fs, permitting the sharing of a single subtraction circuit among the 2N differentiators of the I and Q filters. Figure 8 shows the multiplexed Comb section for a three-stage comb. The Integrator section runs at a sampling rate of $F_{(s\_out)}$. If the circuit clock frequency is at least 2xFs_out, I and Q channels can share each of the N integrators as shown in Figure 9.

2). Comb [3]

A comb filter running at a low sampling rate fs/R, for a rate change of R is an odd symmetric filter described by In the equation, M is a design parameter and is known as differential delay. M is usually limited to 1 or 2. The corresponding transfer function at fs is

$$H_C(Z) = 1 - z^{-RM}$$
(1)

The comb sections are combined with a rate changer. Using a technique for multi-rate analysis of LTI systems the comb sections can be pushed through the rate changer and then become by three things are achieved: Half of the filter has been slowed down and therefore efficiency is increased, The numbers of delay elements required in the comb section have been reduced and The integrator and comb stages are independent of rate changer. The basic structure of a comb is as shown in figure 6.
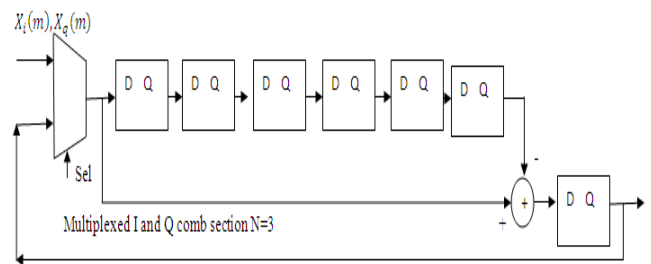

Figure 6: Basic Comb Multiplexed CIC Comb,(N = 3) Stages

3). Integrator

An integrator is a single pole IIR filter with a unity feedback coefficient given by the transfer function for an integrator on the z-plane

$$H_I(z) = \frac{1}{1 - z^{-1}}$$
(2)

The basic structure of an integrator is as shown in figure 7. Design and FPGA Implementation of High Speed, Low Power Digital down Converter for Power Line Communication Systems
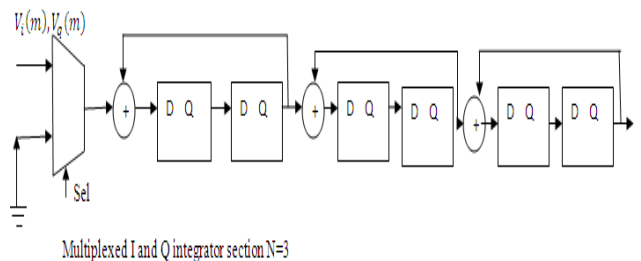

Figure 7: Multiplexed I and Q CIC Integrator Section, N = 3 Stages

4). Frequency Characteristics

The transfer function for a CIC filter at fs is

$$H(z) = H_C^N(z)H_I^N(z) = \frac{(1 - Z^{-RM})^N}{(1 - Z^{-1})^N}$$

(3)

In this equation, N is the number of integrator-comb filter pairs, and R is the rate change factor. Equation 3 implies that the equivalent time domain impulse response of a CIC filter can be viewed as a cascade of N rectangular pulses. Each rectangular pulse has RM taps [3].

5). Features of CIC filters

The CIC filters can take the date and different stages is 1-32-bit Input Data Width, 1-8 Cascaded Stages, 1-2 Cycles Differential Delay, 2 to 16,384 Decimation and Interpolation Sampling Rate can be optionally set minimum and maximum values for the decimator or interpolator rate change factors and enable the rate change factors to be set at run time, Multi-channel (up to 4 Channels) Support for Both Decimation and Interpolation, Fully Synchronous and Single-clock Design.

4. DDS AND MIXER

Direct digital synthesizers (DDS), or numerically controlled oscillators (NCO), are important components in many digital communication systems. Quadrature synthesizers are used for constructing digital down and up converters, demodulators, and implementing various types of modulation schemes, including PSK (phase shift keying), FSK (frequency shift keying), and MSK (minimum shift keying). A common method for digitally generating a complex or real valued sinusoid employs a look-up table scheme. The look-up table stores samples of a sinusoid. A digital integrator is used to generate a suitable phase argument that is mapped by the look-up table to the desired output waveform. A simple user interface accepts system-level parameters such as the desired output frequency and spur -suppression of the generated waveforms.

The DDS element generates a digital representation of sine and cosine waves that are then mixed with either the signal to be up/down-converted. Figure 8 is a simplified block diagram of a phase-truncation implementation of a DDS. The P-bit phase accumulator is used to generate a binary value that selects a single point within the sine/cosine table. The output frequency of the DDS sinusoids is proportional to the rate at which the phase accumulator moves through the table. The phase-accumulator width, P, is determined by the frequency resolution required for the application. Each bit of the phase accumulator represents   sections of the unit circle.
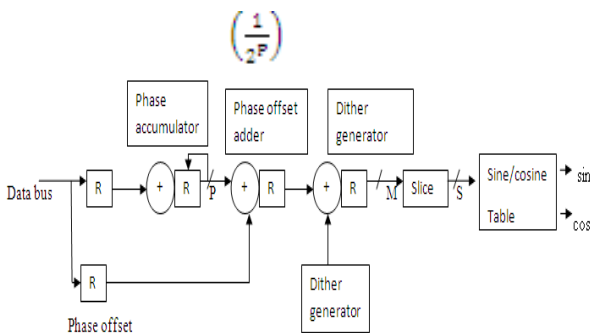

Figure 8: DDS Simplified Block Diagram [6].

Large width phase accumulators provide finer resolution. You adjust the phase accumulation rate through writing increment values into the Phase Increment register. Optionally, the phase can be offset by setting the Phase Offset register to a non-zero value. Normally, the bit width (P) of the phase accumulator is significantly larger than the number of address bits (S) required for the sine/cosine table.

The truncation to S bits introduces errors into the wave generation, creating frequency spurs in the output spectrum. One method of reducing the magnitude of the spurs is by ''spreading'' the error through the introduction of a low-level random signal into the sine table address. The dither generator and adder are used to create a random low-level signal that is mixed into the binary sine/cosine table address to spread the error.

Multi-channel DDS operations are accomplished by cycling through the generation of new phase-accumulator values each clock, one for each channel. The phase accumulator is replaced by an adder followed by a delay element, which acts as the register for each channel.

The delay element stores the accumulated phase value for each channel until that channel's time slot. Then it is incremented by the channel-specific phase increment value being read from the phase increment memory. In this way, the phase accumulator is divided into individual channels. Typically dither is only incremented after all time slots are cycled through. The sine and cosine table values are addressed exactly as in the single-channel case.

5. RESULTS

In this design three individual interpolation filters were cascaded along with a DDS and a mixer into a digital up converter. Coding of the sub-blocks of the main DDC has been implemented using simulink and Xilinx system generator Simulations were carried using Xilinx blocks. System Generator provides a Resource Estimator block that quickly estimates the area of a design prior to place and route. This can be a valuable aid in the hardware / software partitioning process by helping system designers take full advantage of the FPGA resources.

Figure 9: Resource Estimates window in Simulink/System Generator.

Table 1: Frequency Comparison in different stages in DDC

Stages	Sampling rate	Frequency(In fs=3MHz)
CIC Filter	5	600KHz
C(z) filter	2	300KHz
P(z) filter	-	300KHz

DDC has three different decimation stages filters as written in table 1. The first stage of decimation is CIC, in this down sampled by a factor 5. Input frequency is 3 MHz and the output frequency of CIC is 600 KHz the second stage is C (Z) filter, it is down-sampled by a factor 2 and the output frequency is 300 KHz and P (z) filters without any decimator factor.
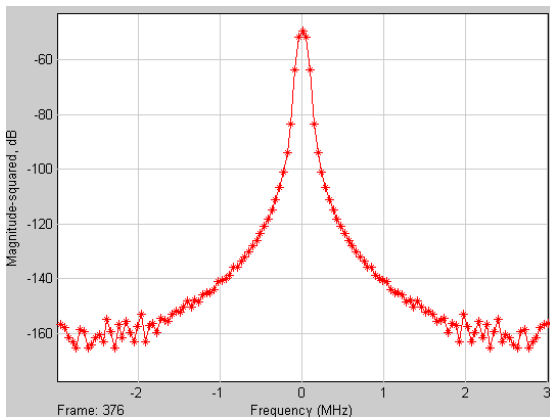

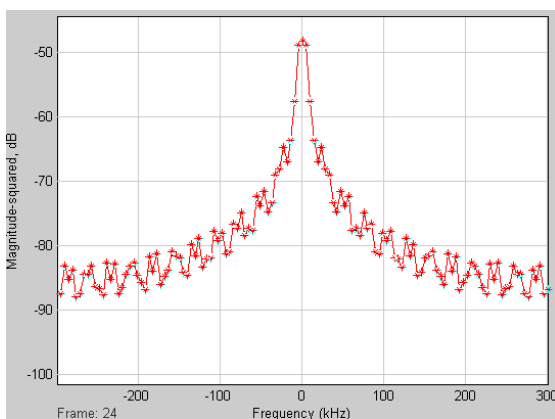**Figure 10 Simulations Input of Wider Bandwidth 6 MHz Frequency.**

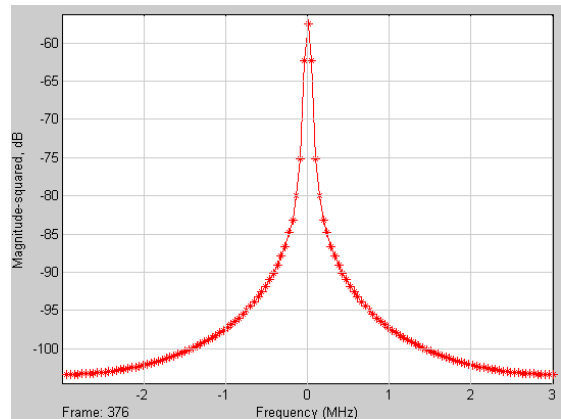**Figure 11 Simulations output of Narrow Bandwidth of 600 KHz Frequency.**

Figure 12 Output from the Hardware co-simulation using Virtex®-5 devices

6. CONCLUSION

With its combination of low unit costs and architecture optimized for DSP functions, Virtex-5 FPGA devices now enable the industry‴s lowest price-points for high-performance DSP functions. Xilinx further enables embedded DSP functions by providing design tools that fit within the standard DSP designer‴s tool flow, and enhances productivity by automating the FPGA implementation process.

With the availability of the Virtex®-5 devices, the associated design tools, and the increasing number of off-the-shelf DSP functions optimized for this fabric, designers must evaluate embedding DSP functions within the Virtex®-5 FPGA as one of the options when designing systems.

REFERENCES

[1] "Physical Layer Standard for cdma2000 Spread Spectrum Systems", Revision D, 3GPP2 C.S0002-D, version 1.0, February13, 2004

[2] D. Babic, J. Vesma, and M. Renfors, "Decimation by irrational factor using CIC filter and linear interpolation," IEEE International Conference on Acoustics, Speech, Signal Processing, May 2001.

[3] E. B. Hogenauer "An Economical Class of Digital Filters for Decimation and Interpolation", IEEE Trans. Acoust., Speech Signal Processing, Vol 29, No 2, pp 155-162, April1981.

[4] P.P. Vaidyanathan, "Multirate Systems and Filter Banks", Prentice Hall, Englewood Cliffs, New Jersey, 1993.

[5] Mohamed Al Mahdi Eshtawie, and Masuri Bin "OthmanAn Algorithm Proposed for FIR Filter Coefficients Representation" World Academy of Science, Engineering and Technology

[6] Direct digital synthesizers (DDS), Xilinx logi core generation April 28, 2005.

[7] Xilinx logi core MAC FIR v5.1 April 28, 2005 Product specification.