Design of 16-bit Vedic Multiplier for Convolutional Encoder using VHDL

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ABSTRACT
In general, multiplication plays an vital role in the development of processors, DSP applications, image processing etc. So, designing of high speed multiplier is a neccesary choice. In this research, design of 4, 8 and 16-bit multiplier based on vedic mathematics has been presented. These multipliers further will be used in the design of convolutional encoder. Here, Urdhava Tiryakbhyam sutra is used for multiplication. It eliminates unwanted multiplication steps and follows a fast multiplication process and achieves a significantly less computation complexity over its conventional counterparts. All the modules are coded in VHDL and simulation done in Xilinx ISE 14.5i.

Keywords
Convolution encoder, Multiplier, Urdhava Tiryakbhyam, Vedic mathematics

1. INTRODUCTION
Vedic multipliers are based on Vedic Sutras. In Sanskrit word 'Veda' stands for 'knowledge'. Vedic mathematics is believed to be reconstructed from Vedas by Sri Bharti Krishna Tirathaji between the years 1911 to 1918. The Vedic mathematics has been divided into sixteen different Sutras which can be applied to any branch of mathematics like algebra, trigonometry, geometry etc. Its methods reduce the complex calculations into simpler ones because they are based on methods similar to working of human mind thereby making them easier. An encoder is a device that converts information from one format or code to another for the purpose of speed. Convolutional encoding is one of the forward error correction scheme. Error correction technique plays a very important role in communication systems. The error correction technique improves the capacity by adding redundant information for the source data transmission. It provides an alternative approach to block codes for transmission over a noisy channel. Convolutional codes are characterized by code rate and memory of the encoder (n,k,K). The code rate is typically given as n/k, where n is the input data rate and k is output symbol rate.The memory is called the "constraint length" 'K' where the output is a function of the previous K-1 inputs. Convolutional codes were introduced in 1965 by Peter Elias. Convolutional codes are used extensively in numerous application in order to achieve reliable data transfer, including digital video, radio, mobile communication and satellite communication. Convolution encoding is a process of adding redundancy to the information sequence which is going to be transmitted over the channel. Redundancy means introducing some extra symbols to the information sequence so that the output bit pattern generated makes the transmitted data more immune to the noise in the channel. A convolution encoder processes the information serially.

2. VEDIC MATHEMATICS SUTRA
Vedic Mathematics deals with Sixteen Sutras. Only one Sutra "Urdhva Tiryakbhyam" has been discussed here.

2.1 Urdhva Tiryakbhyam
This sutra is based on "Vertically and Crosswise" technique. It makes almost all the numeric computations faster and easier. The advantage of multiplier based on this sutra over the others is that with the increase in number of bits, area and delay increases in comparison to others. Here is the example of urdhva tiryakbhyam sutra for binary number system. In Fig.1, this method is illustrated with the multiplication of two decimal numbers 325 and 738. The numbers of steps in the process depend upon the number of the digits being used. Digits on the two ends of the lines are multiplied and resultant is added to the carry from previous step. When the number of crossing lines in a single step is greater than one then they all are added along with the previous carry. After this, only the least significant digit of the resulting number is taken as product digit and rest are considered as carry digits. Initial carry is taken as zero.

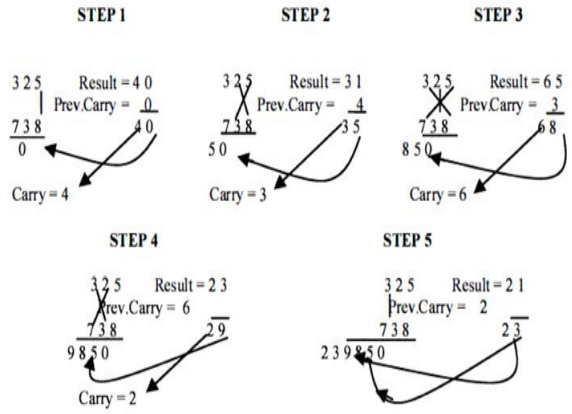

Fig 1: Multiplication of two decimal numbers using Urdhva Tiryakbhyam [7]

Another technique for the calculation of Urdhva Tiryakbhyam method is shown in Figure 2. In this technique, the numbers to be multiplied let us say 5498 and 2314 are written on the consecutive sides of the square table. On partitioning the square into rows and columns, each row/ column belongs to one of the digit of the two numbers to be multiplied such that every digit of one number has a small square common to the digit of other number. These small squares are further divided into two equal parts by crosswise lines. Now the each digit of one number is multiplied with every digit of second number and two digit products are placed in their corresponding square. The digits on crosswise line are added with previous carry. Digits on dotted significant digit of the resulting

number are taken as product digit and rest are considered as carry digits. Initial carry is assumed to be zero here also.

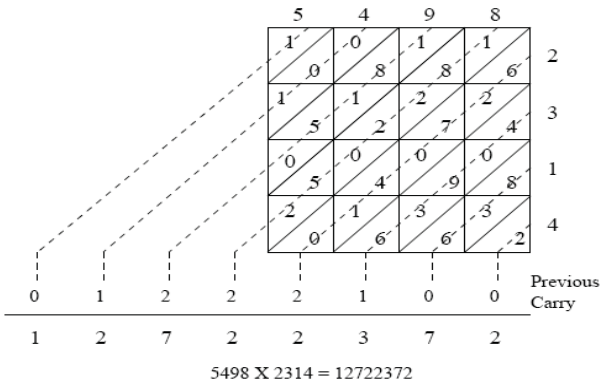

Fig 2: Alternative way to calculate the Urdhva Tiryakbhyam [6]

3. DESIGN OF VEDIC MULTIPLIER

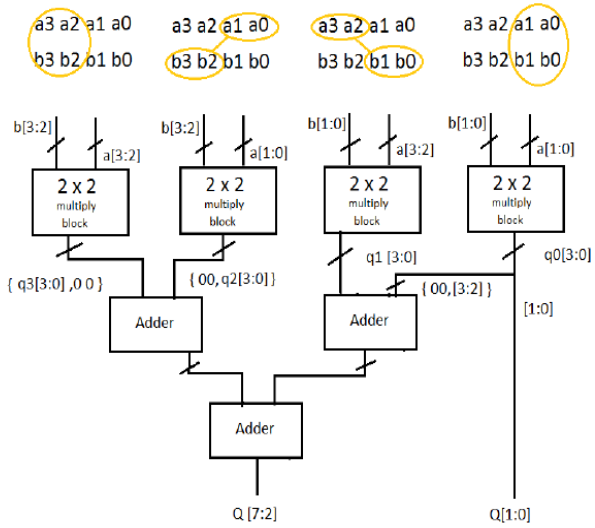

Fig 3: Design of 4x4 multiplier

Using 4 such 2x2 multipliers and 3 adders we can built 4x4 bit multipliers as shown in fig. 3

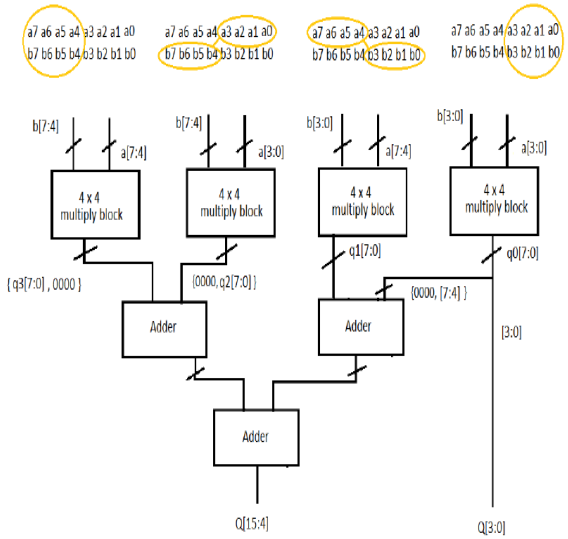

Fig 4: Design of 8x8 multiplier

Similar to the previous design of 4x4 multiplier, we need 4 such 4x4 multipliers to develop 8x8 multipliers. Here we need to first design 8bit and 12 bit adders and by proper instantiating of the module and connections as shown in the fig 4 we have designed a 8x8 bit multiplier

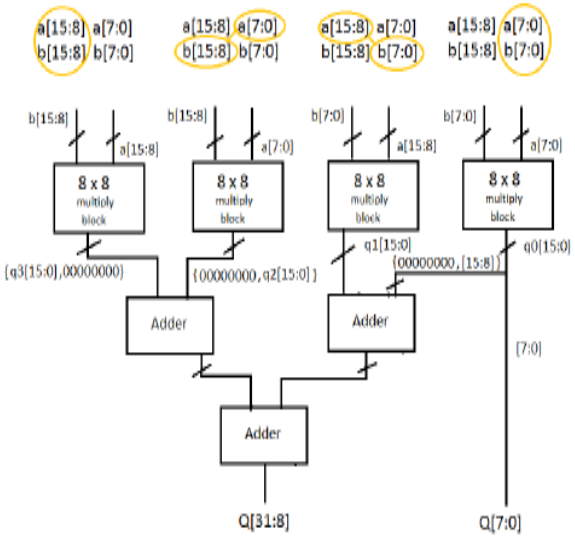

Fig 5: Design of 16x16 multiplier

Using 4 such 8x8 multipliers and 3 adders we can built 16x16 multiplier as shown in the fig 5.

4. EXPERIMENTAL RESULTS

4.1 RTL SCHEMATICS

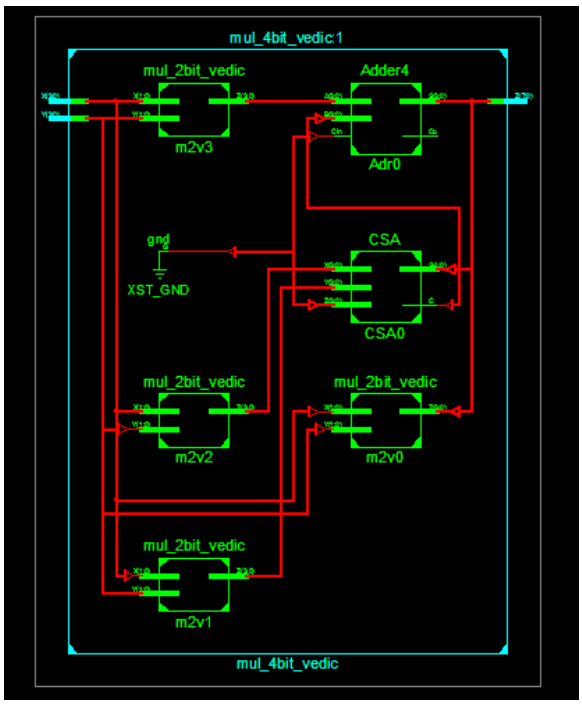

Fig 6: RTL Schematic of 4-Bit Vedic Multiplier

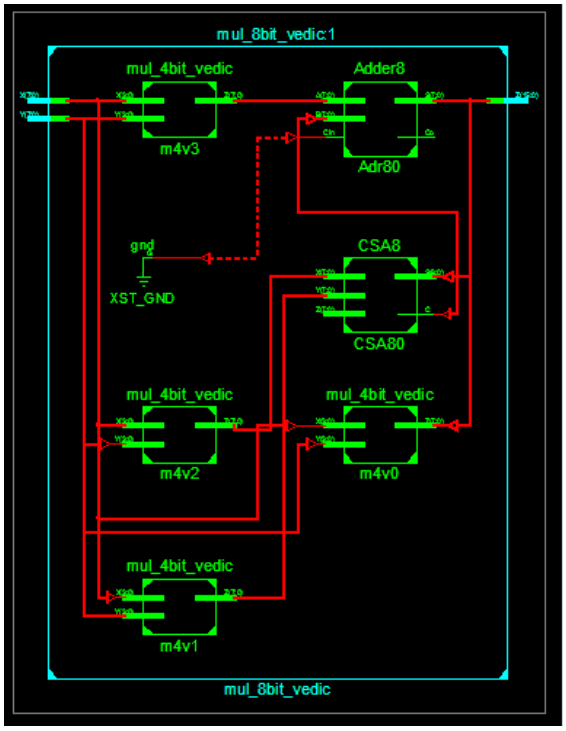

Fig 7: RTL Schematic of 8-Bit Vedic Multiplier

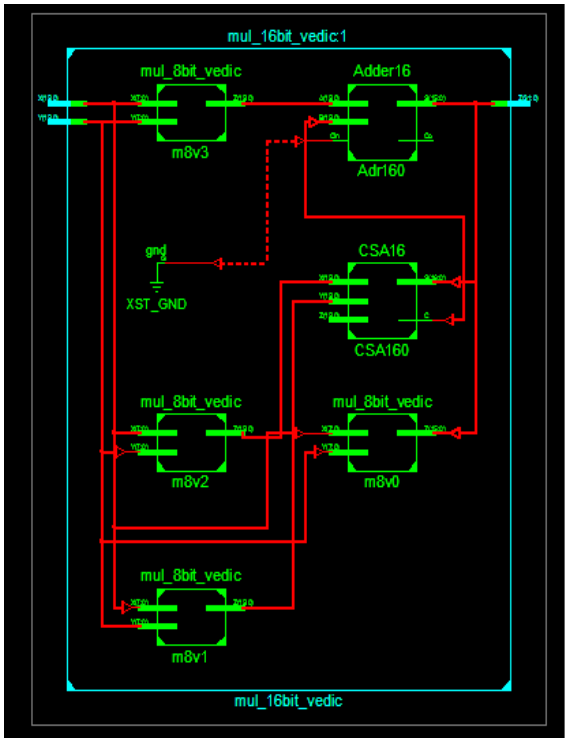

Fig 8: RTL Schematic of 16-Bit Vedic Multiplier

4.2 SIMULATION RESULT

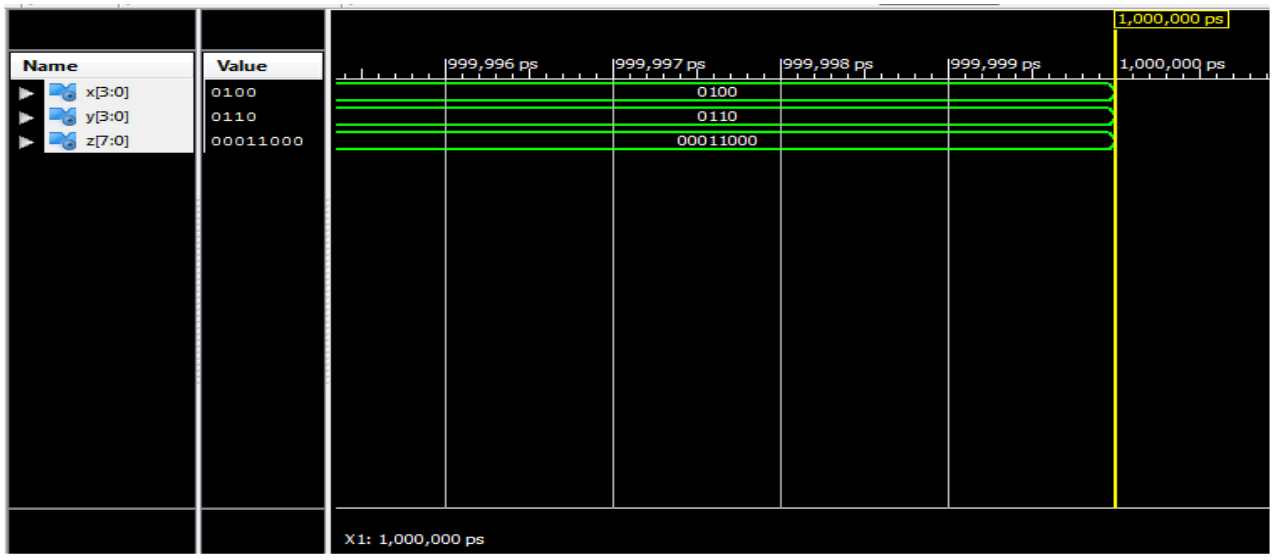

Fig 9: Simulation Result of 4-Bit Vedic Multiplier

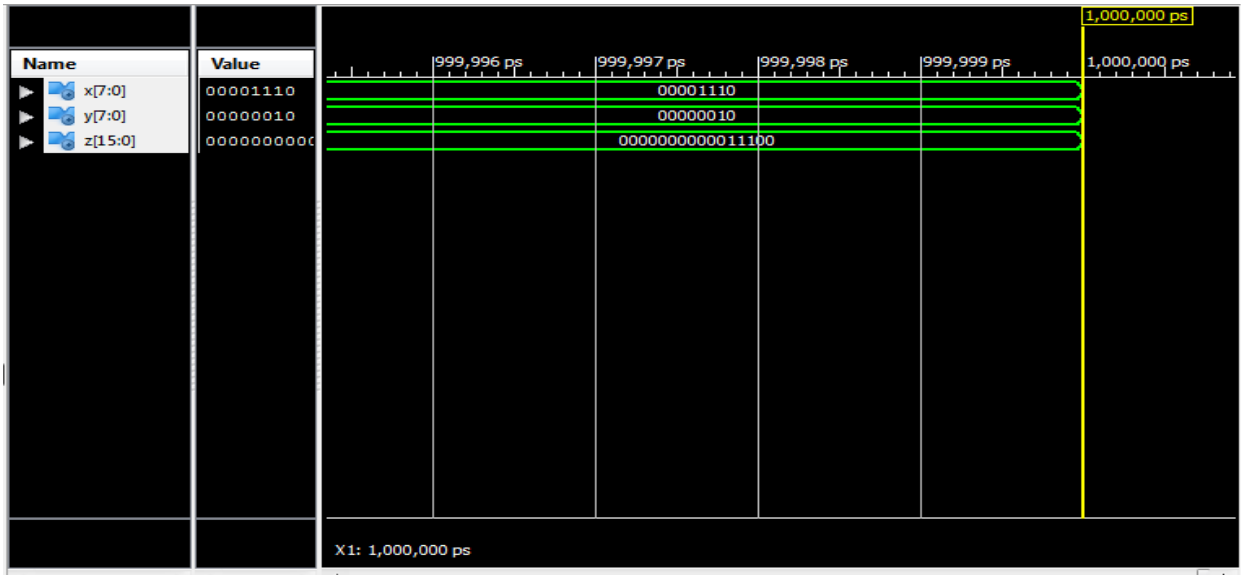

Fig 10: Simulation Result of 8-Bit Vedic Multiplier

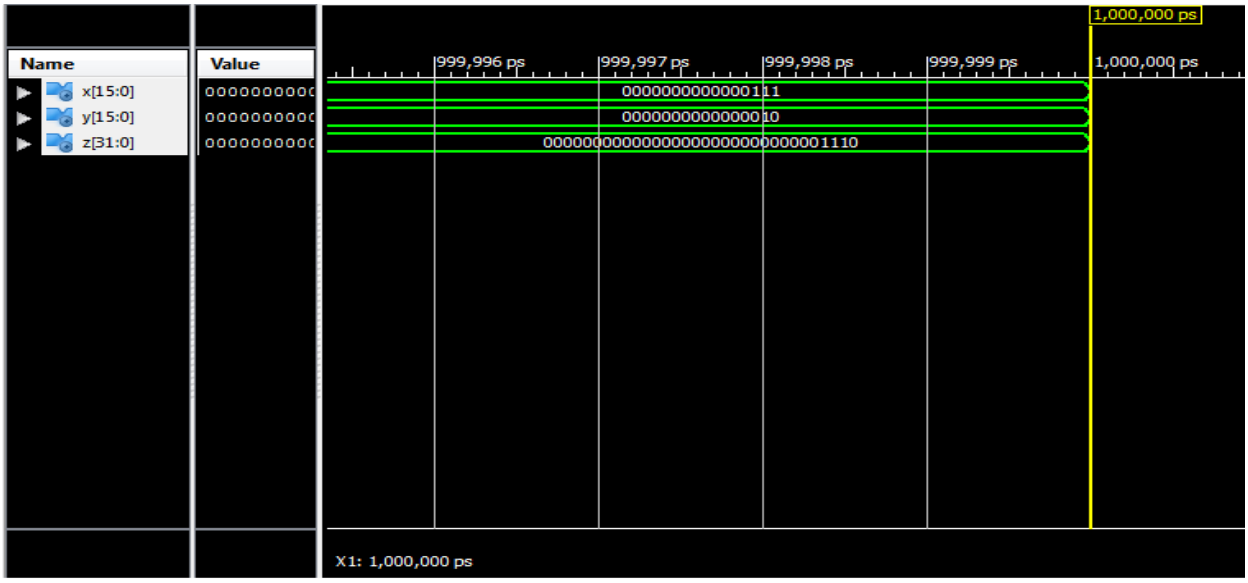

Fig 11: Simulation Result of 16-Bit Vedic Multiplier

Table 1. Synthesis Results

Vedic multipliers	4 Bit	8 Bit	16 Bit
Delay	11.393ns	19.790ns	30.534ns

The delay observed in the table 1 are software (simulation) delay i.e., as we increase the bits of operation delay also increases.

5. CONCLUSION

In this paper, we have presented the design and simulation of 4-bit, 8-bit and 16-bit vedic multiplier.As the size of multiplier increases delay also increases. Here, Urdhava Tiryakbhyam sutra is used for multiplication because it eliminates unwanted multiplication steps and follows a fast multiplication process. The design has been achieved using VHDL and simulated with Xilinx 14.5i. In future work, this multiplier will be used in convolution encoder. The advantages of this proposed architecture is efficient in speed. The multiplier can be extended upto 32-bit, 64-bit etc.

6. REFERENCES

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