Design and Implementation of HDLC Transmitter using VHDL

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ABSTRACT
Data communication over the network is efficiently carried out with the help of protocol. Protocol is set of rules that define the format of frame, packet or message that are exchanged between devices. HDLC i.e. High level data link control protocol is one of the protocol defined by International Organization for Standardization (ISO) for data link layer of OSI reference model. HDLC is bit oriented protocol and widely used in the network. It is used to send the data in proper frame format. This paper discusses the design of HDLC transmitter coded in VHDL and its simulation in Modelsim software.

Keywords-
HDLC, VHDL, FCS, FPGA, Verilog HDL, Xilinx.

1. INTRODUCTION
High level data link control (HDLC) protocol is developed by the ISO for data link layer of OSI reference model. It specifies a packetization standard for serial links. It is mostly used as it supports half duplex, full duplex communication lines, point and multi-point networks. The procedures outlined in HDLC are designed to permit synchronous, code-transparent data transmission. In HDLC protocol, the control information is always in the same position, which reduces the chance of errors. HDLC is bit orientated protocol as it sends information as a sequence of bits. It has also capability of error detection. It is suitable for Frame Relay switches, Video conferencing on ISDN, SONET Termination, X.25 layer-2 protocol, Cable Modem, Private packet data networks & switches.

HDLC is a specification for the Data Link layer and lies between the Physical layer and the Network layer. The Network layer is responsible for passing a packet of data through an internetwork, which can consist of many individual local area networks and even wide area links. The Data Link layer, of which HDLC is a part of, is responsible for passing the data between two nodes on the same network. HDLC takes packets from the Network layer and attaches and address, control, and data integrity information to them. Once formatted, the packets are sent "down the wire" using the Physical layer. Thus in HDLC protocol, the data is arranged in proper frame.

1.1 HDLC frame structure
In this protocol, data is encapsulated in frame which includes address field, control field and FCS. The frame format is shown below-

Flag	Address	Control	Data	FCS	Flag

Fig. 1 HDLC frame format.

(1)Flag- Every frame starts and ends with flag sequence 01111110. At any time, the transmission of frame can be aborted by sending the abort flag which is bit sequence of 01111111. Flags are continuously transmitted on the link between frames to keep the link active.

(2)Address- It is an 8 Bit or 16 bit field. It consists of the address of the receiver.

(3)Control field- It control the communications process. This field contains the commands, responses and sequences numbers used to maintain the data flow accountability of the link, defines the functions of the frame and initiates the logic to control the movement of traffic between sending and receiving stations.

(4)Data or Information-It consists of data i.e. number of bits; the sender actually wants to transmit to the receiver.

(5)FCS-This field contains a 16-bit, or 32-bit cyclic redundancy check bits. It is used for error detection. The fields are transmitted from left to right, least significant bit first.

HDLC uses a technique called bit-stuffing to differentiate bit sequence from a flag field. Every time the user wants to send a bit sequence having more than 5 consecutive 1s, it inserts (stuffs) one redundant 0 after the fifth 1. This extra zero is inserted regardless of whether the sixth bit is another one or not. Its presence tells the receiver that the current sequence is not a flag. Once the receiver has seen the stuffed 0, it is dropped from the data and the original stream is restored. This paper aims to design and implement the HDLC transmitter using VHDL. Here the transmitter is designed and design of receiver is proposed.

2. PROPOSED SYSTEM
From the study of related work [1], it has been seen that HDLC transceiver is designed using VHDL and it is designed to operate at different rate of frequency. When the transceiver is designed at maximum frequency, it can be used in many applications. Thus the research work aims to design Enhanced HDLC protocol using VHDL which includes the design of transmitter and receiver operating at maximum frequency.

2.1 Proposed Model for transmitter
The proposed diagram of transmitter includes blocks of address insertion, FCS generation, Zero insertion block. The block diagram is shown in figure 2.

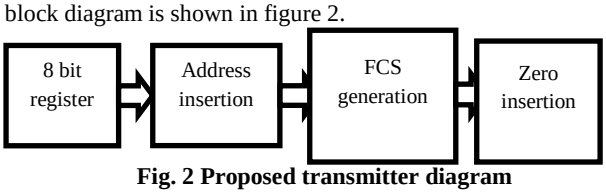

Fig. 2 Proposed transmitter diagram

As seen in figure 2, the data to be transmitted is given to register and parallel to serial conversion is done .Then, address of receiver is added in the data. Address may be 8 bits or 16 bits. After this, FCS bits are added in frame which is used for error detection. In order to avoid the confusion between data and flag bits, zero bits are stuffed when five consecutive ones are detected in data. Then, flag bits 0111110 are added at beginning and end of the frame. In this way, actual data is transmitted after arranging it in frame format.

2.2 Proposed Model for receiver

The design of receiver is proposed and shown in figure 3. It can be implemented in future work.

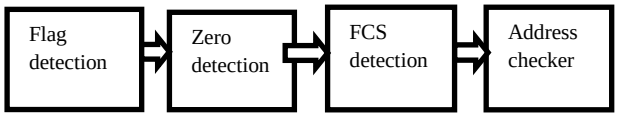

Fig. 3 Proposed receiver diagram

When the frame data is received at receiver, the flag sequence is detected. After that, extra zeros are detected which are added in bit insertion process. After detection of extra zeros, they are removed from the bit sequence. Then FCs bits are detected and receiver will calculate its own FCS bits. When FCS bit sequence are equal, it indicates that transmission is error free. In this way, the error is detected. Then the address is detected and verified. In this way, the whole data is retrieved. The proposed work aims to design protocol at maximum the bit rate thereby making the design more flexible and efficient.

3. DESIGN AND IMPLEMENTATION

The proposed work includes the design of transmitter and receiver for HDLC protocol. Out of the two main modules, transmitter is designed and implemented. Following figure 4 shows the basic block diagram of HDLC transmitter. The main blocks of transmitter are-1. 8-bit register- Transmit register module is responsible for capturing the data on the rising edge of clock signal.

2. Address insertion-This block contains the address of the destination, which can be either of 8 bits or 16 bits address. This can be any arbitrary address, or the broadcast or "All-Stations" Address, which are all one.

3. FCS generation-FCS is performed for detecting errors in the received data by grouping the bytes of data into a block and calculating a Cyclic Redundancy Check (CRC). The CRC is calculated by performing a modulo 2 division of the data by a generator polynomial and recording the remainder after division and that remainder is FCS. In software, it is basically performed using a shift register and X-OR gates. This method is used for generating the FCS bits in design of the transmitter.

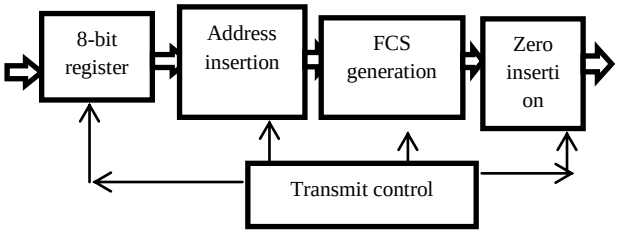

Fig. 4 Block Diagram of transmitter.

4. Zero insertion- When the bit sequence having more than 5 consecutive 1s is detected, this block inserts (stuffs) one redundant 0 after the fifth 1.

5. Transmit control -HDLC Transmitter controller is responsible for generating all the necessary internal control signals.

When the system is initialised, the data and address is loaded on rising edge of the clock signal and reset signal is high. After the loading of whole data, the FCS bits are included the frame data. FCS i.e Frame Check Sequence is sequence of bits that are appended in data for error detection. It is calculated by using 16/32 bit Cyclic Redundancy Check (CRC) method. Extra zeros are inserted by the bit stuffer into the bit stream to avoid transmission of the control flag sequences within the frame data. This method of adding the zeros is called bit stuffing or transparency. This operation involves inserting a zero after any sequence of 5 consecutive ones in the transmitted data stream. Its presence tells the receiver that the current sequence is not a flag. Once the receiver has seen the stuffed 0, it is dropped from the data and the original stream is restored. In this way, the data is transmitted. Each module of the HDLC transmitter is modelled, simulated and synthesized using VHDL. Finally all the blocks were integrated using port mapping technique in VHDL in order to get the complete HDLC Transmitter. The design is successfully implemented in Modelsim SE 6.2c software.

4. SIMULATION RESULT AND ANALYSIS

The simulation result of implemented HDLC transmitter is shown in figure 5. The design is coded in VHDL and successfully implemented in ModelSim SE 6.2c software. This software from Mentor Graphics is the tool used for pre-synthesis and post-synthesis simulation. VHDL language is used as it can describe the behaviour and structure of electronic systems, but is particularly suited as a language to describe the structure and behaviour of digital electronic hardware designs, such as ASICs and FPGAs as well as conventional digital circuit.

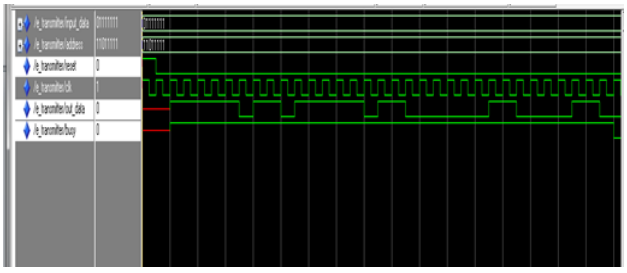

Fig. 5- Simulation result of transmitter

As seen from figure 5, initially the input data 01111111 and address 11011111 is loaded on rising edge of clock signal and reset signal is high. When reset becomes zero, the whole data including input data, address, FCS bits and flag sequence starts transmitting. The out_data line indicates the flow of bits that are transmitting. The busy line indicates whether the transmission is completed or not. When busy line is 1, the transmission is going on and when it is 0, the transmission is completed. At the transmitter side, the bits of frame that are transmitted is 11111 0 11 11111 0 110 000001100001100.

5. RESULT

The design is coded in VHDL and successfully implemented in Modelsim SE 6.2c. The transmitter is found to be running at 31.25Mbps. The final implementation of proposed HDLC transceiver will be done on Xilinx software by selecting the suitable family of FPGA.

6. CONCLUSION

The transmitter for HDLC protocol has been successfully implemented in Modelsim SE 6.2c software. The coding for transmitter is done in VHDL language. Each module of the transmitter is thoroughly simulated before and after synthesis. For increasing the efficiency of transmitter, it can be implemented in Xilinx suit of software. Thus this paper describes the design and implementation of HDLC transmitter using VHDL. This project can be used in MODEMS where error detection part is performed by this HDLC controller and also it can be used in other communication network.

7. FUTURE SCOPE

As the proposed work involves the design of transmitter and receiver, receiver can be designed in this paper. Both transmitter and receiver can be designed to operate at higher frequency to achieve the aim of research work. By increasing the bit rate, its efficiency will be increased and it can be used in more application. Thus making the HDLC controller more efficient, flexible and upgradable.

8. REFERENCES

[1] Rupal P. Bende,.A.P.Bagade, Prof.S.R.Salwe," Review on Design of HDLC Protocol using HDL", International Journal of Innovative Research in Electrical, Electronics, Instrumentation and control engineering, Vol. 4, Issue 2, February 2016.

[2] Syed Manzoor Qasim and Shuja A. Abbasi *," FPGA Implementationof a Single-Channel HDLC Layer-2 Protocol Transmitter using VHDL"*, International Conference on Electrical, Electronics and System Engineering, 2003.

[3] S. Hamed Javadi and Ali Peiravi*,"Design and Implementation of a High Bit Rate HDLC Transceiver Based on a Modified MT8952 Controller",* Australian Journal of Basic and Applied Sciences,2009.

[4] K.Sakthidasan, Mohammed Mahommed*,"Design of HDLC Controller Using VHDL"*, International Journal of Scientific & Engineering Research Volume 2, Issue 3, March-2011.

[5] Harpreet Singh, Navneet Kaur, Vinay Chopra and Dr. Amardeep Singh*," Optimization of multi - channel HDLC protocol transceiver using Verilog"*, International Journal of Computer Science Issues, Vol. 9, Issue 2, No 2, March 2012.

[6] Armaan Hasan Nagpurwala,Sundaresan C, Chaitanya CVS*, "Implementation of HDLC Controller Design using Verilog HDL "*, International Conference on Electrical, Electronics and System Engineering,2013.

[7] Gaurav Chandil, Priyanka Mishra*,"Design and Implementation of HDLC Controller by Using Crc-16",* International Journal of Modern Engineering Research (IJMER) Jan.-Feb. 2013.

[8] Jai Karan Singh1, Mukesh Tiwari, Mohd Firoz Warsi*,"Implementation of HDLC Protocol Based DDR-RAM Radar Processing System"*, International Journal of VLSI and Embedded Systems-IJVES -May - June 2013.

[9] Shubham Fadnavis*,"An HVD Based Error Detection and Correction Code in HDLC Protocol Used for Communication",* International Journal of Advanced Research in Computer and Communication Engineering, Vol. 2, Issue 6, June 2013.

[10] Shashank Rampelly, Santhosh Rao Seri, Gnaneshwara Chary, Krishanm Raju, *"Data Communication Using HDLC Protocol",* International Journal of Innovative Research in Electrical, Electronics, Instrumentation and control engineering ,Vol. 2, Issue 5, May 2014.

[11] Gao, Zhen-bin and Jian-Fei Liu,*"FPGA implementation of a multi-channel HDLC protocol transceiver"*, In Proceedings of the 2005 International Conference on Communications, Circuits and Systems,2: 1300-1302,2005.

[12] Lu, Y., Z. Wang, L. Qiao and B. Huanq, "*Design and implementation of multi-channel high speed HDLC data processor,"* IEEE International Conference on Communications, Circuits and Systems, and West Sino Expositions, 2: 1471-1475,2002.

[13] Jun Wang; Wenhao Zhang; Yuxi Zhang; Wei Wu; Weiguang Chang; Sch. of Electron. & Inf. Eng., Beihang Univ. (BUAA), Beijing, China "*Design and implementation of HDLC procedure based on FPGA"* , Anti-counter feiting, Security, and Identification in Communication, ASID, 3rd International Conference, 20-22 Aug.2009.

[14] Wang Lie, Yi Mingvol, "*Design of HDLC Controller based on XILINX FPGA* ", International Conference on Electrical, Electronics and System Engineering IEEE, 2011.