Performance Analysis of VLSI Floor planning using Evolutionary Algorithm

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ABSTRACT
Floorplanning is an important physical design step for hierarchical, building-block design methodology. When the circuit size get increases the complexity of the circuit also increases. To deal with the increasing design complexity the intellectual property (IP) modules are mostly used in floorplanning. This paper presents a Hybrid particle swarm optimization algorithm for floorplanning optimization. Here B*tree is used at the initial stage in order to avoid overlapping of modules and later, PSO algorithm along with the concept of crossover and mutation from Genetic algorithm is used to get optimal placement solution. The main objective of floorplanning is to minimize the chip area and interconnection wire length. The Experimental results on Microelectronic Center of North Carolina (MCNC) benchmark circuits shows that our algorithm performs better convergence than the other methods.

General Terms
Floorplanning, Very Large Scale Integrated Circuits(VLSI)

Keywords
Hybrid particle swarm optimization (HPSO), Genetic algorithm (GA), Crossover, Mutation, Microelectronic Center of North Carolina (MCNC), Very Large Scale Integrated Circuits(VLSI)

1. INTRODUCTION
As the demand for latest technology surge in the market, more research has been carried out in the field of IC design, which in turn makes VLSI design developed with more composite, reliable, compact and better performance. As the number of transistors in a single chip is countless, the IC design has become much more complex. A more sophisticated approach to the above problem is Floorplanning, which is an important physical design step for hierarchical, building-block design methodology. When the circuit size get increases, the solution space also increases simultaneously which make it impossible to find the global solution space. The HPSO algorithm can be adopted to solve floorplanning problem.

Recently, many researchers resort to stochastic optimization algorithms based on slicing [8] and non-slicing floorplan [10,9,4]. In [10][9], bounded slicing grid and sequence pair approaches were used to represent non-slicing floorplan with smaller solution space. Both these approaches use constraint graph to manipulate the transformation between the representation and their placement. But it is more complicated. To overcome the above problem pei-Ning Guo et al.[6] proposed an O-tree representation based on non-slicing floorplan. Experiment results shows that this representation achieves minimum wire length and very less dead space. Yun-Chih Chang et al., [3] present an efficient, flexible and effective data structure, B*tree based Simulated annealing schemes for representing non-slicing floorplans. This representation runs about 4.5 times faster than the O-tree, and consumes about 60% less memory and also achieves near optimum area utilization even for rectilinear modules Finally, like O-tree, the size of the search space of the floorplanning problem by the B*tree representation is only $O(n^{2^{n-2}/n!^{2}})$ [3], while it is $O(n^{n/2})$ by the sequence pair representation [14]. Hence, the B*-tree representation is adopted in this paper.

Since VLSI floorplanning is NP-hard, different heuristic methods have been proposed. They are classified into two methods: the constructive method and the iterative method. The constructive method use heuristic strategy to construct a floorplan. The bottom-left (BL) and BL fill methods [2] are the most common constructive approaches. Huang et al. [7] presented a very effective heuristic algorithm, in which two important concepts, namely, the corner-occupying action and caving degree, were introduced to guide the packing process. The iterative method use metaheuristic approach such as simulated annealing, tabu search, genetic algorithm and particle swarm optimization algorithm to produce final best solution. Jianli Chen et al. [4] proposed a new heuristic method that uses a hybrid simulated annealing to represent non-slicing floorplan. In [13], a genetic algorithm was applied to tackle the VLSI floorplanning problem. In [1] S. Anand et al., proposed a new algorithm named as Simulated Spheroizding Annealing Algorithm (SSAA) which is more suitable for problems of larger size floorplans. In [8] W-L. Hung proposed genetic algorithm based thermal-aware floorplanning. This is the first paper considered thermal-aware floorplanning but it consider only one constraint area and it obtains the final fittest solution.

The particle swarm optimization (PSO) was developed by James Kennedy and Russell Eberhart in 1995. It is an stochastic optimization technique based on the movement and swarm intelligence.PSO is initialized with the population of random solution and it applies the concept of social interaction to problem solving. Unlike most of other population-based evolutionary algorithms, PSO is motivated by the simulation of social behaviour instead of the survival of the fitness. The advantages of PSO are simplicity in implementation and its ability of convergence is very quick,(Sun et al. 2006) originally introduces PSO into the floorplanning problem. The paper adopts the B*-tree floorplanning structure (Chang et al.2000) to generate an initial stage with overlap free for placement and utilizes PSO to find out the potential optimal placement solution. However, no implementation detail of the algorithm is mentioned, and only the area optimization is considered. It is unable to solve problems that optimize the area and wire length simultaneously, thus it is not an effective PSO algorithm for
3. **B^*TREE REPRESENTATION**

This paper presented B^* tree based representation at the initial stage to avoid overlapping of modules. The main advantage of using B^*tree is it handles non-slicing structure which is flexible to deal with hard modules in O(n) times. The procedure to construct B^* tree is similar to the depth first search (DFS), while constructing B^* tree, the first priority is given to construct the left sub tree followed by right sub tree in repetitive fashion, with its root representing the bottom left corner in the floorplan and thus the coordinate of the module is (x_{root}, y_{root})=(0,0). Let n_i be the root node, and n_j be either left or right node. If node n_j is the left child of root node n_i, module j is placed on the right hand side which is adjacent to the module i, i.e., x_{j} = x_{i} + w_i, where w_i is the width of the module i. Similarly if node n_j is the right child of root node n_i, module j is placed above the corresponding root node with the constraint x_j=x_{i}

![Image](a) Admissible placement (b) B^*tree representing the placement

Since n0 is the root node in figure 3 (b), the module b0 is placed on the bottom left corner. Then based on the DFS procedure n7 is the left child of n0, so the module b7 is placed on the right hand side of b0.Since there is no left sub-tree exist after the node n7, it starts to construct right sub-tree of node n7 (i.e n8).This procedure continues until all the nodes in the tree are constructed in the recursive manner. The above construction takes only linear time.

4. **HYBRID PARTICLE SWARM OPTIMIZATION**

4.1 **Particle Swarm Optimization**

Particle swarm optimization (PSO) is an optimization method that optimizes a problem by iteratively trying to improve a candidate solution with regard to a given measure of quality. PSO optimizes a problem by having a population of candidate solutions (from b^*tree). The individuals in the population are called as particles. By using PSO algorithm the particles are moved around in the search-space according to simple mathematical formulae over the particle’s position and velocity. Each particle’s movement is influenced by its current velocity and the particle’s position which is known as its local best known position and is also guided toward the best known positions in the search-space, which are updated as better positions are found by other particles. This is expected to move the swarm towards the best solutions. The velocity and position of each particle is updated according to the following equation (1) and (2).

$$V_{id} = W \times V_{id}^{t-1} + C_1 r_1 (P_{id} - X_{id}^{t}) + C_2 r_2 (P_{gb} - X_{id}^{t})$$  \hspace{1cm} (1)

$$X_{id}^{t} = X_{id}^{t-1} + V_{id}^{t}$$  \hspace{1cm} (2)

![Figure 1: Slicing floorplan and its slicing tree](a) Slicing floorplan (b) Slicing tree

**2.2 Floorplan Structure**

Floorplan can be represented in two ways, namely, slicing and non-slicing floorplan. The slicing structure can be bisected horizontally or vertically on recursive basis till each part contains only one module. Non-slicing floorplan cannot be bisected in this manner. In fig 1: (a) letter denotes modules and number denotes horizontal and vertical cut division. Figure 2 shows a non-slicing floorplan and the number in the Figure 2 denotes the number of modules in the floorplan. This paper considered non-slicing based floorplan representation.
where \( t \) is the iteration index, \( d \) is the number of dimensions (variables), \( w \) is the inertia weight, \( c_1 \) and \( c_2 \) are two positive constants, called acceleration constants, \( r_1 \) and \( r_2 \) are two random numbers within the range \([0,1]\). Equation (1) calculates a new velocity for each particle (potential solution) based on its previous velocity \( (V_G^{t}) \) and the personal best location \( P_{gd} \) or \( P_{gd} \) which the particle has achieved so far and the global best location \( P_{gd} \) or \( gBest \) of the population. Equation (2) updates \( i^{th} \) particle’s position in solution hyperspace. Acceleration coefficient of each particle is calculated using equation (3) and (4).

\[
C_1 = c_1 \times \text{random} \times (x_{gbest} - x_G) + x_G \quad \text{(3)}
\]

\[
C_2 = c_2 \times \text{random} \times (x_{gbest} - x_G) + x_G \quad \text{(4)}
\]

where \( c_1 \) and \( c_2 \) are the current iteration number and MAXITER is the maximum number of allowable iteration, \( c_1, c_2 \) represent the final value of the \( c_1 \) and \( c_2 \) and \( c1, c2s \) represent the initial values of the \( c_1 \) and \( c_2 \).

### 4.2 Genetic Algorithm

Genetic algorithms are computational procedure that mimics the natural process of evolution. The objective of the GA is to find an optimal solution to a problem. Inspired by the GA, a PSO algorithm with crossover and mutation operators for the floorplanning problem is proposed.

#### 4.2.1 Crossover and Mutation

Two point crossover operator [11] is used in this paper. In figure 4 two crossover points are selected randomly from particle 1. An element from starting of the particle 1 to the first crossover point is copied to the new particle and then the elements are selected randomly from particle 2 for the crossover point and copied in new particle and then the rest is copied from particle 1. For mutation operator, a element is selected randomly and its direction is changed.

![Crossover points](image)

**Fig 4:** The crossover operator

### 4.3 Fitness Evaluation

In PSO each particle corresponds to a potential solution, therefore, a layout can be obtained after decoding the particle. Usually, the objective of the optima is to minimize the chip area or wire length of floorplanning. Considering the minimization of area, the fitness is equal to the value of area. Thus the fitness function for area can be represented as follows:

\[
f(x) = W(x) \times H(x) \quad \text{(5)}
\]

where \( W(x) \) is the width of the corresponding particle \( x \), and \( H(x) \) is the height of the particle \( x \). For multi-objective optimization the fitness function can be represented as

\[
g(x) = \lambda_1 \times f(x) + \lambda_2 \times t(x) \quad \text{(6)}
\]

where \( \lambda_1 \) and \( \lambda_2 \) are constant weights, \( f(x) \) is the area of particle \( x \), \( t(x) \) is the wire length of particle \( x \) which is calculated by using HPWL(Half-perimeter wire length). It is defined as half-perimeter length of the smallest bounding box that encloses all pins. The HPWL of the \( p^{th} \) net can be calculated according to the equation (7)

\[
L_p = X_{max} - X_{min} + Y_{max} - Y_{min} \quad \text{(7)}
\]

where \( X_{max} \) and \( X_{min} \) are the maximum and minimum x-coordinate of the HPWL bounding box of the net, \( Y_{max} \) and \( Y_{min} \) are the maximum and minimum y-coordinate of the HPWL bounding box of the net. The total wire length can be calculated using equation (8)

\[
t = \sum_{p=1}^{m} L_p \quad \text{(8)}
\]

### 4.4 Algorithm Description

**STEP 1:** Load modules data and initialize the parameter of the PSO algorithm

**STEP 2:** Generate an initial population, initialize the position and velocity of each particle, and calculate the Pbest of each particle and the Gbest population

**STEP 3:** calculate the fitness value of each particle by equation (5) and (6)

**STEP 4:** Check each particle, if its fitness value is better than Pbest, update its Pbest with the fitness value

**STEP 5:** Check each particle, if its fitness value is better than population’s Gbest, update its Gbest with the fitness value

**STEP 6:** Adjust the position and velocity of each particle according to equations (1) and (2)

**STEP 7:** If termination condition is satisfied, the algorithm stops; otherwise, go to step 3.

### 5. EXPERIMENTAL RESULTS

#### 5.1 Parameter Settings for Algorithm

All the cells are set as hard IP modules. The parameters of the PSO algorithm are set as follows: \( W=0.95 \), \( C1 \) decreases linearly from 0.82 to 0.5 and \( C2 \) increases from 0.4 to 0.83. The probability of crossover set as 0.85 and mutation as 0.005. The population size is set as 10 and the maximum number of generation is 10,000.

<table>
<thead>
<tr>
<th>CIRCUIT</th>
<th>MODULES</th>
<th>NETS</th>
<th>I/O</th>
<th>PAD</th>
<th>PINS</th>
</tr>
</thead>
<tbody>
<tr>
<td>APTE</td>
<td>9</td>
<td>97</td>
<td>73</td>
<td>287</td>
<td></td>
</tr>
<tr>
<td>XEROX</td>
<td>10</td>
<td>203</td>
<td>2</td>
<td>698</td>
<td></td>
</tr>
<tr>
<td>AMI33</td>
<td>33</td>
<td>123</td>
<td>42</td>
<td>522</td>
<td></td>
</tr>
<tr>
<td>AMI49</td>
<td>49</td>
<td>408</td>
<td>22</td>
<td>953</td>
<td></td>
</tr>
</tbody>
</table>

### 5.2 Performance of Algorithm

Consider the standard MCNC benchmark circuits APTE, XEROX, HP, AMI33 and AMI49. The simulation programs are implemented in MATLAB. Each benchmark circuit has standard number of modules, nets, i/o pad and pins. The characteristics of MCNC benchmark circuits [5] are shown in table 1.
The figure 5, 6, 7, 8 shows that the area and wire length are optimized simultaneously. The table 2 shows the comparison between HSA and HPSO.

Table 2. Comparison between HSA and HPSO

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Apte</th>
<th>Ami33</th>
<th>Ami49</th>
<th>xerox</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Area (mm²)</td>
<td>Wire (m)</td>
<td>Area (mm²)</td>
<td>Wire (m)</td>
</tr>
<tr>
<td>HPSO</td>
<td>47.44</td>
<td>263</td>
<td>1.29</td>
<td>58.4</td>
</tr>
<tr>
<td>HSA</td>
<td>47.12</td>
<td>480</td>
<td>1.21</td>
<td>61.2</td>
</tr>
</tbody>
</table>
From table 2, it can be seen that in terms of area utilization and wirelength, the proposed algorithm performs better results than HSA. In HPSO, the wirelength was reduced considerably, though there is a small increase in area for the benchmark circuits apte, ami33 and ami49. Hence both wirelength and area have been optimized.

6. CONCLUSION AND FUTURE WORK

Very large-scale integrated floorplanning is NP-hard in combinatorial optimization problem. To solve it in an efficient way, a HYBRID PSO algorithm was proposed. Traditional PSO algorithms often show weakness in solving discrete problems, the proposed algorithm can overcome this weakness in some degree. The experimental results for MCNC benchmark circuit demonstrated that the proposed algorithm can achieve the optimal and reasonable solution for the hard IP modules placement. The future work will focus on the parameter related to thermal-aware floorplanning.

7. REFERENCES


