In GaAs/GaAsSb Heterojunction TFET

Arathy Varghese M.TechScholar, Department of Electronics and Communication Engineering, SAINTGITS College of Engineering, Kottayam, India, Praveen C.S. M.TechScholar , Department of Electronics and Communication Engineering, SAINTGITS College of Engineering, Kottayam, India,

ABSTRACT

Tunnel FETs are a promising alternate to MOSFETs for low power design due to the ability to scale threshold voltage and hence supply voltage, without increase in OFF currents. However, they suffer from low ON currents. Demonstrated here is theenhancement in ION in arsenide-antimonide staggered-gap heterojunction (hetj) tunnel field-effect transistors (TFETs) by engineering the effective tunneling Moderate-stagger height Ebeff. barrier GaAs0.4Sb0.6/In0.65Ga0.35As and high-stagger GaAs0.35Sb0.65/In0.7Ga0.3As hetj TFETs are analyzed, and their electrical results are compared with the In0.7Ga0.3As homojunction (homj) TFET. The GaAs0.4Sb0.6/In0.65Ga0.35Ashetj TFET achieves 134% enhancement in ION over the In0.7Ga0.3As homj TFET at VDS = 0.5 V. With electrical oxide thickness (Toxe) scaling from 2.3 to 2 nm, and using a high staggered hetero junction the enhancement further increases to 285%, resulting in a record highION of 135 µA/µm.

Index Terms

Band to band tunnelling, GaAsSb, InGaAsSteep Subthreshold slope

1. INTRODUCTION

IN n-TFETs, carrier injection relies on the band-to-band tunneling (BTBT) of electrons from a degenerate p+ source into the intrinsic channel conduction band, so that high-energy carriers are filtered out by the semiconductor bandgap, thereby achieving steeper subthreshold slopes. Tunneling field-effect transistors (TFETs) can achieve a sub-60 mV/decade switching slope at room temperature and thus enable supply voltage scaling [1], [2] and [3]. III–V-semiconductor-based heterojunction TFETs are of interest as they allow a high on–off current ratio (I_{ON}/I_{OFF}) and high I_{ON} through reduction in the tunneling barrier height [4], [5].Further performance can be improved by incorporating barrier engineering in hetjTFET for simultaneouslyoptimizing the ION/ IOFF and average subthreshold slope.

1.1 MOTIVATION AND LITERATURE REVIEW

The major limitations of MOSFET include high leakage current, subthreshold slope limitations and tunneling currents. A device with steeper SS would have its I_{DS} modulated over orders of magnitude with a smaller change in V_{GS} . For the same V_{DD} , a device with a smaller SS would achieve a lower I_{OFF} for a given I_{ON} . Both dynamic and standby power consumption can thus be reduced. The intensively studied are steep subthreshold devices are, FINFETs, Impact ionization MOS transistor (I-MOS),

1.1.1 TFET

Ancy P. Mani M.TechScholar, Department of Electronics and Communication Engineering, SAINTGITS College of Engineering, Kottavam, India, Ajith Ravindran Assistant Professor , Department of Electronics and Communication Engineering, SAINTGITS College of Engineering, Kottayam, India

Although the principle of band-to-band tunneling was already discovered in 1957 by L. Esaki, 1958 and the first gated p-i-n structure was proposed in 1978, the interest in the first results on TFETs was limited. This changed rapidly after W. Hansch and I. Eisele et al. started to investigate the TFET in 2000 and J. Appenzeller et alfound in 2004 that the TFET might provide a means to overcome the 60 mV/dec switching limit of the classical MOSFET.

1.1.2 TFET Structure

TFET structure is similar to MOSFET, but with opposite type doping in Source and Drain. The simplest TFET is a gated P-I-N diode where the source and drain are highly doped with the gate controlling the band-to-band tunneling between the Ichannel region and the P+ or N+ region by way of energy band bending in the I-channel In order to be consistent with MOSFET technology [6], the names of the device terminals are chosen such that voltages are applied in a similar way for Tunnel FET operation..

Simulation showed that by reducing only the bandgap of the TFET material from Si to InAs or InSb, the ION increases by several orders of magnitude and can be reached at lower electric fields. Recent experimental results for InGaAs TFETs indicate that a higher ION at a lower VG than with Si TFETs seems possible [7]. The first InGaAs TFET by Mookerjeaet al. achieved an on current of 20 µAµm-1 with an S of 250 mV per decade, whereas Zhao et al.(2009) [8] improved ION to 50 μ A μ m-1 with an S of around 90 mV per decade, which is the best local swing achieved so far for III-V-based TFETs but is still above the thermal limit of MOSFETs. The degraded S is attributed to parasitic tunneling mechanisms involving traps in the source tunnel junction. A few studies have reported on the integration of high-K dielectrics with an antimonide such as GaSb with focus on the lower part of the bandgap between the midgapand the valence band,[9,10,11]whereas mixed arsenide/antimonideshave not been addressed.

The effective bandgap for tunneling can be decreased even further by using hetero structures. Although there is not yet full agreement on whether a staggered or a broken gap alignment works best, all theoretical studies predict that the TFET performance can be significantly enhanced compared with homjs. To reduce the tunneling barrier, InAs and GaAsSb were chosen for the source, with AlGaSb and InGaAs for the channel. Another reason for selecting these materials is that they allow lattice-matched growth, and thus the use of conventional III–V growth and processing technologies.

1.2 INGAAS/GAASSB HETEROJUNCTION TFET

Tunneling field-effect transistors can achievea sub-60 mV/decade switching slope at room temperature and thus enable supply voltage scaling. [1], [2] and [3] III-Vsemiconductor-based hetj TFETs are of interest as they allow a high on-off current ratio (I_{ON}/I_{OFF}) and high ION through reduction in the tunneling barrier height. A wide range of tunable effective barrier heights (Ebeff) [6] can be achieved with mixed As-Sb based hetj TFETs. An In0:7Ga0:3As/GaAs0:35Sb0:65 n-channel hetjTFET with proper bandgap engineering is believed to attain a MOSFETlike on current of 135 µA/ µm and a high ION/IOFF ratio of 10^4 at a drain bias voltage (V_{DS}) of 0.5 V.

1.2.1 Proposed System

The proposed system is a bandgap engineered heterojunction TFET having material composition as shown in the figure 1. This system is found to overcome the low on current trade off of other TFETs by providing an ON current similar to that of MOSFET without compromising for the steep subthreshold slope of TFETs.



Figure 1: Barrier Engineered Arsenide-AntimonideHetj TFET



Figure 2: (a) and (b) Cross-sectional schematics of (a) GaAs0.4Sb0.6/In0.65Ga0.35As moderate hetj and (b) GaAs0.35Sb0.65/In0.7Ga0.3Ashigh hetj TFET (c) and (d) Energy band diagrams showing band alignment [5]

The drive current enhances on replacing an InGaAshomjTFET by a hetjInGaAs/GaAsSbhetj.Further enhancement can be attainedbyengineering the effective tunneling barrier height Ebefffrom 0.58 to 0.25 eV [13, 14]. Moderate-stagger GaAs0.4Sb0.6/In0.65Ga0.35As and highstagger GaAs0.35Sb0.65/In0.7Ga0.3As hetj TFETs are considered, and their electrical results are compared with the In0.7Ga0.3As homiTFET (Ebeff = 0.58 eV). Due to thereduction in Ebeff, the GaAs0.35Sb0.65/In0.7Ga0.3As hetj TFET achieves enhancement in ION over the In0.7Ga0.3Ashomj TFET at VDS = 0.5V. Withelectrical oxide thickness (Toxe) scaling from 2.3 to 2 nm, the enhancement further increases, resulting in a record high ION of 135 uA/umatVDS=0.5V. Mixed lattice-matched heterojunctions(GaAsxSb1-x/InyGa1-yAs) provide a wide range of compositionally tunable Ebeff[4]. With increasing Sb and In compositions, Ebeff can be reduced from 0.5 eV (x = 0.5, y = 0.53) to 0 eV (x = 0.1, y = 1), and hence, the TFET ION can approach the MOSFET level without compromising the steep switching [13] and high ION/IOFF property desirable in a lowpowerlogic switch.

Table 1 Modeling The Proposed System Using Mathematical Equations

Device Type	Homojn TFET	Moderatestagger ed Heterojn TFET	High StagerredHete rojn TFET
Eb(eff)	0.58	0.31	0.25
Toxe(nm)	2.3	2	2
VDS	0.5	0.5	0.5
$\lambda(nm)$	4.4	4.0	3.5
MR	0.017	0.019	0.022

Tunnel FETs utilize a MOS gate to control the band-to-band tunneling across adegenerate p-n junction. The schematic cross-section and energy band diagrams of nchannelTFET in OFF and ON states are shown in When zero bias is applied to gate, conduction band minimum of channel is above the valence band maximum of the source, so band-to-band tunneling is suppressed. A tunneling window, qVtw, opens up as conduction band of the channel is shifted below the valence band of the source. Electrons in the valence band with energy in this tunneling window tunnel into empty states in the channel transistor ON. and the is



Figure 3: Schematic cross-section and energy band

As shown in Figure 3 c when the gate bias is negative, the valence band maximum of the channel can be shifted above the conduction band minimum of the drain leading to electron tunneling from the channel into the drain [6]. Therefore, the tunneling window opens up again, with the tunnel junction

shifted from the source channel junction to the drain-channel junction. When this happens the channel conduction changes from one carrier type to another and the transfer characteristic is said to be ambipolar. This behavior is generally universal across TFET geometries.

1.3 DRAIN-SOURCE TUNNELING CURRENT

The central expression in the TFET model is an experimentally well-established equationfor band-to-band, Zener tunneling in planar *p*-*n* junctions, the primary transport mechanism in tunnel transistors. The two-terminal Zener tunneling behavior is then generalized to three terminals by introducing physics-based expressions for the biasdependenttunneling window *Vtw* and a dimensionless factor *f*, which accounts for thesuperlinear current onset in the output characteristic. $I_{dt}(V_{gs}, V_{ds}) = afEV_{tw}e^{-b/E}$ (1)

Here a and b are given by,

$$a = \frac{WTCHq^3}{8\pi^2\hbar^2} \sqrt{\frac{2m^*}{E_g}} \text{and}b = \frac{4\sqrt{2m^*E_g^3}}{3q\hbar} \qquad (2) \quad \text{Where} mr^* =$$

 $(1/me^* + 1/mh^*)$ -1 is the reduced effective mass, which is the sum of thereciprocal of the electron, me^* , and hole, mh^* , effective masses, Egis the

semiconductorband gap, and \hbar is the reduced Planck's constant.

Figure 3a and b. The device is normally off. diagram of an nchannel TFET when the device is biased in (a) OFF (b) ON and (c) ambipolar state

$$m_r^* = MRm_0 (3)$$
$$E_a = EG_a a (4)$$

The factor f is given by,

$$f = \frac{1 - e^{-\frac{V_{dse}}{GAMMA}}}{1 + e^{\frac{(V_{thds} - V_{dse})}{GAMMA}}} (5)$$
$$V_{dse} = V_{dsmin} \left[\frac{V_{ds}}{2V_{dsmin}} + \sqrt{DELTA^2 + \left(\frac{V_{ds}}{2V_{dsmin}} - 1\right)^2} - \sqrt{DELTA^2 + 1} \right] (6)$$

 $V_{dsmin} = 10^{-15}$

$$V_{thds} = LAMBDA \tanh(Vgs)$$
 (7)

The parameter Vdseapproaches zero as

*Vds*becomesnegative. The electric field in the tunneling junction is given by

$$E = E0(1 + R1V_{ds} + R2V_{goe})$$
 (8)

Vgoealso approaches zero as Vgobecomes negative,

$$V_{goe} = V_{min} \left[1 + \frac{v_{go}}{2v_{min}} + \sqrt{DELTA^2 + \left(\frac{v_{go}}{2v_{min}} - 1\right)^2} \right]$$
(9)

Vmin=0.0001

The tunneling window is given by

$$V_{tw} = \ln(1 + e^{V_{gt}/U})$$
 (10)

The Urbach factor U is considered to be a linear function of gate voltage

$$U=R0U_0+(1-R0)U_0V_{goen}$$
 (12)

$$U_0 = VtN1$$
 (13)

Where

$$V_t = \frac{k_b(temp+273.15)}{q}$$
(14)
$$V_{goen} = \frac{V_{goe}}{V_{TH}}$$
(15)

Parameter Extraction in Q1

The fitting methodology used to select the parameters is outlined as follows. Theparameters in the table can be grouped between physical and adjustable.

The n-channel moderate-stagger and highstaggerhetj TFETs are analyzed and compare their electrical results with the In0.7Ga0.3As homj TFET (Ebeff= 0.58 eV)[16]. By scaling Ebeff, with the electrical oxide thickness (Toxe) being 2.3 nm, we demonstrate enhancement in drive current at V_{DS} = 0.5 V V_{OFF} being the gate voltage corresponding to *I*OFF = 5 nA/ μ m. By further scaling Toxe to 2 nm, the enhancement in drive current is further more.

2. ANALYSIS AND OBSERVATIONS



Fig 1. N-Channel Homojunction TFET

 I_{ON} =0.035mA/µm =35µA/µm and I_{ON}/I_{OFF} =7*10³

 $I_D\text{-}V_{DS}$ Characteristics of homojunction TFET is obtained as shown and here it attains an ON current of $35\mu A/\mu m$.But this ON current is much lower than the MOSFET but provides a high I_{ON}/I_{OFF} of $7*10^3$



Fig 2. N-Channel Moderate Staggere Heterojunction TFET

 $I_{ON}=0.082 \text{mA}/\mu\text{m}=82 \mu\text{A}/\mu\text{m}$ and $I_{ON}/I_{OFF}=1.64*10^4$

On using a moderate staggered system the I_{ON} has increased to $82\mu A/\mu m$. This shows 134% enhancement in the drive current. This heterojunction based system provides a higher ION/IOFF of $1.6*10^4$.



Fig 3. N-Channel High Stagerred Heterojunction TFET

 $I_{ON}\!\!=\!\!0.135 mA/\mu m$ and $I_{ON}\!/I_{OFF}\!\!=\!\!2.7{*}10^4$

Record ON current is obtained here that is 135 μ A/ μ m on using a highly staggered heterojunction TFET .The ON current obtained here is same as that of MOSFET with a very low OFF current of 5nA/ μ m which raises the I_{ON}/I_{OFF} to 2.7*10^4 without making any compromise in the steep subthreshold slope.All these are attained at V_{DS}=0.5V and room temperature,so the system provides for supply voltage scaling

 $I_{D}\text{-}V_{GS}$ Characteristics of GaAs0.35Sb0.65/In0.7Ga0.3As TFET



Fig 4. Log I_D-V_{GS}Characteristics of GaAs0.35Sb0.65 /In0.7Ga0.3As TFET

The subthreshold slope is measured from the ID-VGS characteristics plotted hereThe effective SS is obtained as

SSeff = $(V_{\text{TH}} - V_{\text{OFF}})/(\log(I_{\text{TH}}I_{\text{OFF}}))$ [6] between V_{OFF} and V_{TH}

Where V_{TH} = (V_{GS}+V_{OFF})/2[17].The subthreshold slope obtained is less than 60 mV/decade for the high hetjTFET at V_{DS} of 0.5V



Fig 5. Log I_D -V_{GS}Characteristics of GaAs0.35Sb0.65 /In0.7Ga0.3As TFET

This makes it possible to use it in high speed switching devices .The comparison between the switching slopeON current and the current ratio of the homj,moderateand high staggered hetj TFET is given in the observation table below.

3. OBSERVATIONS AND RESULT

It is observed that on replacing the InGaAshomjTFET by a moderate staggered heterojunction TFET the $I_{\rm ON}$ is enhanced to $82\mu A/\mu m$ which shows a 134 % enhancement in the current.Tox scaling can also be introduced to obtain further enhancement .When a high staggered hetjis used further improvement is found in drive current and $I_{\rm ON}$ becomes $135\mu A/\mu m$ which shows 285% enhancement in the drive current.

	Homo Junction TFET	Mod.Stager redHeteroj n. TFET	High StagerredHe terojn. (Proposed System)
I _{ON} (μΑ/μm)	35	82	135
I _{ON} /I OFF	7*10 ³	1.64*10 ⁴	$2.7*10^4$
SS(m V/deca de)	65	49.86	37.5

Table 4.1 ON Current Ratio And Subthreshold Table 1.Slope For Homojunction And Heterojunction TFET

4. CONCLUSION

In0.7Ga0.3As homj control, GaAs0.4Sb0.6/ In0.65Ga0.35As moderate-stagger, and GaAs0.35Sb0.65/ In0.7Ga0.3As high stagger hetj TFETs have been analyzed and dependence of $I_{\rm ON}$ on effective tunneling barrier height Ebeff has been systematically studied. $I_{\rm ON}$ enhancements over n-channel Homj-TFET are experimentally demonstrated by utilizing i) a moderate staggered and ii) a high staggered Hetj-TFET. Both techniques show above 100% enhancement in drive current over Homj-TFET .Furthermore, using Toxe scaling in conjunction with Ebeff engineering, a record high ION = 135 μ A/µmalong with the highest ION/IOFF = 2.7 \times 10 to the power 4 in the category of TFETs is achieved at VDS = 0.5 V

5. REFERENCES

- Sakurai T. Perspectives of low power VLSI's. IEICE Trans. Electron E87-C, 429–436, 2004.
- [2] Bernstein K., Cavin, R. K., Porod, W., Seabaugh A. C. &Welser, J. Device and architectures outlook for beyond CMOS switches. Proc. IEEE 98, 2169–2184, 2010.
- [3] AM. Ionescu and H. Riel: Nature 479 329, 2011.
- [4] Knoch J. &Appenzeller, J. Modeling of highperformance p-type III–V heterojunction tunnel FETs. IEEE Electron Device Lett. 31, 305–307, 2010.
- [5] D. Mohata, S. Mookerjea, A. Agrawal, Y. Li, T. Mayer, V. Narayanan, A.Liu, D. Loubychev, J. Fastenau, and S. Datta: Appl. Phys. Express 4 024105, 2011.
- [6] Luisier M. &Klimeck, G. Simulation of nanowire tunneling transistors: from the Wentzel–Kramers– Brillouin approximation to full-band phonon-assisted tunneling. J. Appl. Phys. 107, 084507, 2010.
- [7] Mookerjea S. et al. Experimental demonstration of 100 nm channel length In0.53Ga0.47As-based vertical interband tunnel field effect transistors (TFET) for ultra lowpower logic and SRMA applications. IEEE Int. Electron Devices Meet. 137.1–137.4, IEEE, 2009.
- [8] Zhao H. et al. InGaAs tunneling field-effect transistors with atomic-layer-deposited gate oxides. IEEE Trans. Electron Devices 58, 2990–2995, 2011.
- [9] D.Mohata .et.al Low-Temperature Atomic-Layer-Deposited High-k Dielectric for p-Channel In0:7Ga0:3As/GaAs0:35Sb0:65 Heterojunction

Tunneling Field-Effect Transistor. Applied Physics Express 6 (2013) 101201

- [10] R.M Wallace et al. "Fermi level unpinning of GaSb using plasma enhanced atomic layer deposition" Applied Physics Lett.97
- [11] Wang .C et al. Electrochem.Solid State Lett.15 (2012)H51
- [12] R.Gandhi ,Z.Chen,N.Singh,K Banerjee and S Lee, "Vertical Si nanowire n-type tunneling FETs with low subtreshold swing (<50mV/decade)at room temperature, IEEE Electron Device Lett, vol .32 no.4,pp(437-439) April 2011.
- [13] S. M. Sze and K. K. Ng, Physics of Semiconductor Devices, 3 ed., John Wiley & Sons, INC., 2006
- [14] Verhulst A. et al. Complementary silicon-based heterostructure tunnel-FETs with high tunnel rates. IEEE Electron Device Lett. 29, 1398–1401, 2008.
- [15] Knoch J. Optimizing tunnel FET performance–impact of device structure, transistor dimensions and choice of material. Int. Symp. VLSI-TSA 45–46, IEEE, 2009.
- [16] Boucart K. &Ionescu, A. M. Length scaling of the double gate tunnel FET with a high-κ gate dielectric. Solid State Electron. 51, 1500–1507, 2007.
- [17] A Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," Proc. IEEE, vol. 98, no. 12, pp. 2095–2110, Dec. 2010

6. AUTHOR PROFILE

Ms. Arathy Varghese Pursuing M.Tech Degree in VLSI & Embedded Systems from Mahathma Gandhi University, Kottayam, India. Received B.Tech. Degree in Electronics and communication Engineering from Kerala University, Trivandrum, India, in 2013. Her areas of interests include device modeling and Digital design of VLSI circuits.

Mr. AjithRavindran received the B.Tech and M.Tech. Degrees in ECE from Mahathma Gandhi University, Kottayam, India, in 2010 and 2012 respectively He has been with the Department of ECE, Saintgits College of Engineering, Kottayam, since 2012, where He is currently an Assistant Professor. His current research interests include low-power VLSI systems, and device modelling

Mr. Praveen C S PursuingM.Tech Degree in VLSI & Embedded Systems from Mahathma Gandhi University Kottayam, India. Received B.Tech. Degree in Electronics and Communication Engineering from Mahathma Gandhi University, Kottayam, India, in 2012 His areas of interests include device modeling, low power design of VLSI circuits.

Ms. Ancy P Mani Pursuing M.Tech Degree in VLSI & Embedded Systems from Mahathma Gandhi University, Kottayam, India. Received B.Tech. Degree in Electronics and communication Engineering from Mahathma Gandhi University, Kottayam, India, in 2013. Her areas of interests include device modeling and Digital design of VLSI circuits