Comparator Design for Delta Sigma Modulator

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ABSTRACT
In wide band communication systems, low power and high speed ADCs forms the main building blocks. These ADCs are commonly seen in the front end of the radio frequency receivers. Comparators are used in these ADCs. A CMOS Comparator design, based on amplifier-push pull inverter circuit is elaborated in this paper, which is intended to be used as the 1-bit ADC required for the implementation of a first order Delta Sigma (Δ∑) A/D converter. This particular design for the comparator makes it faster and lowers the power dissipation. This design is realized in both 180 nm and 90 nm CMOS processes using Cadence Virtuoso platform and low power dissipation is found in 90 nm implementation with 1.2 V supply voltage. In this work simulation results are reported and comparison of comparator in both technologies are observed

General Terms
Digital-to-Analog conversion

Keywords
Comparator, Delta Sigma ADC, Delta Sigma modulator, Flash ADC DAC

1. INTRODUCTION
By using CMOS technology millions of transistor can be integrated on a single IC chip. The advancement of VLSI design resulting high speed, less power consumption, effective use of space[1]. Since the real world is purely analog in nature ADCs are unavoidable components in communication systems to interface the analog signal to the digital signal processing core. In addition to speeding up of the design cycle, the DSP core imparts more flexibility and programmability to the design of entire communication system. Also the digital processing makes it more immune to noise and easy to store. Thus in modern digital communication systems the ADC block plays a vital role. Design of ADCs when attempted using CMOS Technology results in low power dissipation, low cost of production and enhanced yield For wireless application Delta Sigma (Δ∑) ADCs are commonly used, because of their dynamic range and low power consumption [2]. An N-bit flash ADC architecture requires 2N-1 comparator [3]. For single bit ADC only one Comparator is required. Design of a 1-bit ADC using the CMOS Comparator applicable for wide band DSM is attempted here in this paper [4].

2. DELTA-SIGMA A/D MODULATOR
An N-bit flash ADC architecture requires 2^N-1 comparator [3]. For single bit ADC only one Comparator is required. Design of a 1-bit ADC using the CMOS Comparator applicable for wide band DSM is attempted here in this paper [4].Analog to digital converters are used while processing the data. The system that converts continuous physical quantity to digital value is analog-to-digital converter [6]. Delta Sigma (Δ∑) ADC is one of the important A/D converters in modern wireless transceivers. It was introduced in 1962. Initially Delta modulators were used, which is based on quantizing the change in the signal from sample to sample rather than absolute value of signal at each sample. Delta Sigma modulator (DSM's) is a improved one of Delta modulator, obtained by shifting the position of loop filter in the feedback path to the feed forward path [7]. Sigma Delta modulator provides high resolution and large bandwidth as demanded by the wide band mobile communication system of the present era, i.e., 3G and even to the 4G system [8]. The block diagram of a first order Delta Sigma modulator is pictured in Fig. 1.

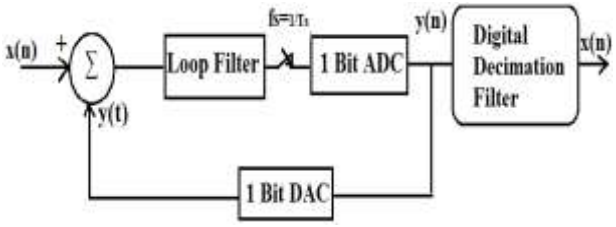

Fig1: Block Diagram of First Oder Delta Sigma A/D Converters

The signal recovery by employing Delta Sigma (Δ∑) ADC is achieved in two steps. First the analog signal is converted to the digital form and then a digital decimation filter is used to generate an accurate representation of the input contribution at the output sample. The Decimator recovers the narrow band signal from the high frequency data stream generated by the Delta Sigma ADC [9].There are mainly two types of Delta Sigma modulators (Δ∑M's) available-Continuous time Sigma Delta modulator (CTΔ∑M) and Discrete time Delta Sigma modulator (DTΔ∑M). Among them, Continuous time DSM is widely used for wideband applications for many reasons including the built in anti-aliasing property and ability to operate at higher

frequency than its respective discrete time counterpart. Also it exhibit high resolution and signal bandwidth [7]. Delta Sigma modulators (∆∑M's) are commonly used at the front end of the radio frequency receivers for filtering the incoming signal by using low pass loop filter. This low frequency signal is fed in to the digital signal processor. The analog to digital conversion includes two procedures - sampling and quantization. The sampling makes the signal discrete in time and quantization makes the signal discrete in amplitude. According to sampling theory, the ADCs are designed to sample the signal at a rate little faster than the nyquist frequency. Oversampling and noise shaping are the two primary characteristics of delta sigma ADCs. The Figure. 2 show the concepts of oversampling and noise shaping.The Sigma Delta modulator makes use of the oversampling of the input signal along with noise shaping to achieve a very high SNR value as compared to the Nyquist rate data converters. The SNR expression for a first order delta sigma converter is given in (1)

SNR = 6:02ENOB + 1:76 + 10 log (OSR) (1)
Where, SNR= Signal to noise ratio
ENOB= Effective number of bits
OSR= Over sampling ratio

2.1 Oversampling

Oversampling is explained by employing the Nyquist sampling theorem. It states that the exact recovery of a signal from its samples is possible if and only if the sampling frequency is greater than or equal to the Nyquist sampling rate, which is twice the value of maximum frequency component present in the Continuous time signal. The ∆∑M's use a sampling frequency much greater than the Nyquist sampling rate which helps in spreading the quantization noise to an extended band, due to high sampling rate, while preserving the signal integrity

2.2 Noise Shaping

Even though the oversampling spreads the quantization noise to an extended band, still the signal component and noise component are in separably mixed. The noise shaping characteristics pulls the quantization noise to band of frequencies well outside the band of interest, i.e., the signal band.

The loop filter is used to realize this property, i.e., the Continuous time loop filter inside the ADC loop offers a Signal Transfer Function (STF), which just delays the input signal and a Noise Transfer Function (NTF) which pulls the quantization noise out of the signal band.

2.3 The CT Delta Sigma Modulator

The general architecture of Continuous time Delta Sigma modulator (CTDSM) is shown Fig. 3. The Delta Sigma modulator (DSM) is composed of four components, an analog difference node, loop filter, 1 bit ADC and 1 bit feedback DAC. The modulator output has only one bit of information. The input signal x (t) and the quantized output y (n) is given to the difference amplifier, whose output is given as the input to the loop filter. The feedback D/A converter is perfect and neglecting the signal delays, the input to loop filter which is the difference between input signal and feedback signal is equal to quantization error.

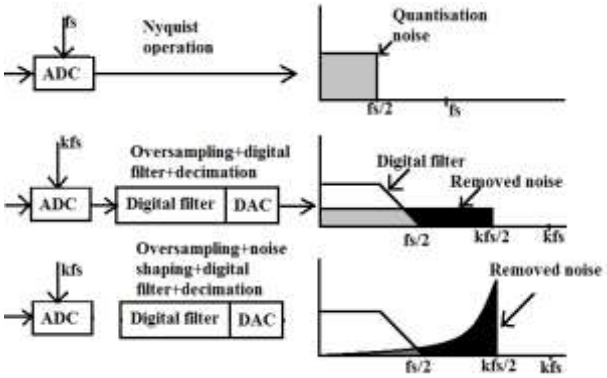

Fig 2: Oversampling and Noise Shaping

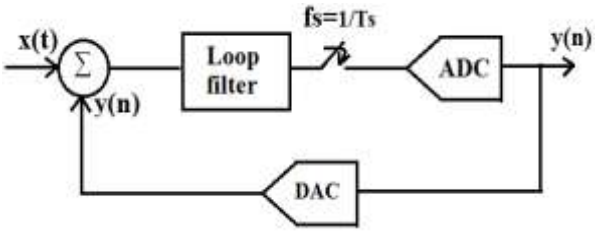

Fig 3: Continuous Time Sigma Delta Modulator

This error is summed up in the loop filter and then quantized by 1 bit A/D converter. The output of Sigma Delta modulator loop gives +1 or -1, which can be averaged over several input sample periods to produce very precise results. The averaging is performed by the decimation filter.

3. FLASH CONVERTERS

In the case of communication system, data conversion plays a major role. The ADC circuit is found in almost all mixed signal integrated circuitsMany different types of ADC architectures are available, each of them having some unique properties. For the application in wireless communication flash ADCs can be used [10]. Mainly these flash ADCs are used, when large bandwidth is available [11]. Flash analog to digital converters are the fastest way to convert an analog signal to digital signal because of its parallel structure.The ADC designed here is for Sigma Delta modulator. Delta Sigma modulators (∆∑M) can be used for wide band communication application, and also where it demands high speed and low power analog to digital converter. There are many different types of ADCs available, among them flash ADC is the most popular because of its conversion rate and accuracy. Comparators are the major component of flash ADC [12]. Another component of flash ADC is the thermometer to binary encoder. The opamp itself can be used as a Comparator. For an N-bit converter the circuit requires 2^N -1 comparators. Here the comparator is designed for single bit higher order Delta Sigma modulator. For single bit ADC only one comparator is required

4. COMPARATOR

In flash ADC, the most important analog component is comparator. Comparator performs the actual conversion in flash ADC. Basically comparator is a 1-bit analog to digital converter [3]. The symbol of comparator is shown Fig. 4Accuracy and speed are the two important design aspects of comparator. Comparator is one of the key blocks for high speed operation. Here the design of Delta Sigma modulator (DSM), single bit ADC is used. The first step of analog to digital conversion process is sampling the input. To obtain the digital output of analog signal, the sampled signal is fed to the comparator. The working of the Comparator is such that, when the applied analog input voltage is higher than the reference voltage comparator produces output as 1. If the input voltage is less than the reference voltage, output is 0. The main function of the comparator is to compare the applied input signal voltage with the reference voltage.

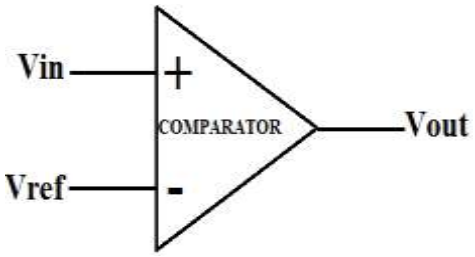

Fig 4: Symbol of Comparator

The comparator is the one of the important subcomponents of ADCs. Its optimization is important because it limits the speed of the converter. Comparator can be designed in different models, such as latch based comparator, pre-amplifier latch with clock driven circuit etc. These circuit also exhibit high resolution, data rate, low power dissipation etc but it contains much more number of transistors, which increases the circuit complexity. In order to minimize the number of transistors, here an open loop comparator is used. The Comparator here used consists of input stage, push-pull inverter and output stage. The input stage contains an amplifier-single stage opamp. The opamp itself can act as a comparator. The application of this amplifier stage in the comparator design is to amplifies the input signal thereby improving the comparator sensitivity [13]. In this comparator circuit, latches are not used. When latches are used it affect, the resolution, and also an additional amplifier is requiredfor amplifying the latch output, which makes circuit more complex.

The fig. 5 show the circuit diagram of Comparator. The transistor PM0, PM4, NM0, NM1 makes amplifier stage. Where PM0 and PM4 are the load transistors, and NM0 and NM1 are the input transistors. The structure consisting of transistors NM2 and NM3 forms the current mirror [14].

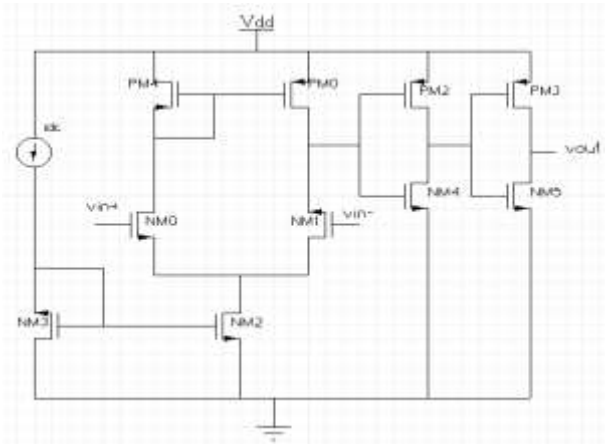

Fig. 5: Circuit Diagram of Comparator

The mirror circuit is used because the design of current source in analog circuit is based on copying current from a reference, with the assumption that one precisely defined current source is already available. Here a stable reference current IREF is applied, which is copied to many current sources in the system. After the input stage a push-pull inverter is used, which is a type of electronic circuit that uses a pair of active devices that alternatively supply current to, or absorb current form, a connected load. Push-pull circuits are used in many amplifier output stages. For reducing the capacitive effect an ideal inverter with least W/L ratio can be used. By using this open loop comparator circuit area can be reduced, since the number of transistors used is small.

5. SIMULATION RESULT AND DISCUSSION

5.1 Comparator output

Table 1 shows the transistor sizing of the comparator. Simulation result of comparator which is done in both 90 nm and 180 nm CMOS technologies are reported here. For 90 nm CMOS technology a supply voltage of 1.2 V and for 180 nm CMOS technology 2.5 V is used as supply voltage. The schematic diagram of comparator in 90 nm and 180 nm technology is shown in Fig. 6 and Fig. 7 respectively.

Table 1:Transistor size of the comparator

Technology	90 nm	180 nm
pmos width(nm)	120	2000
pmos length(nm)	100	180
nmos width(nm)	120	2000
Nmos length(nm)	100	180

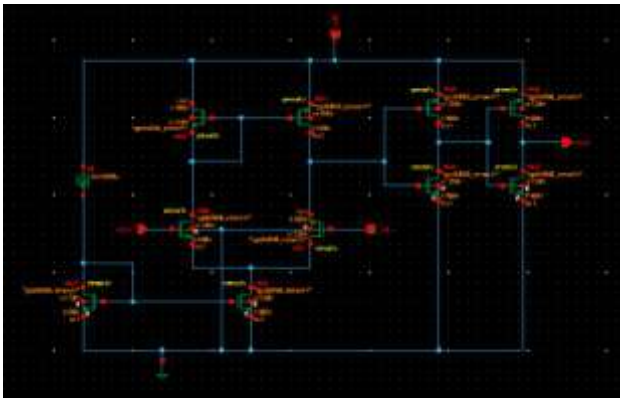

Fig 6: Schematic Diagram of Comparator in 90 nm Technology

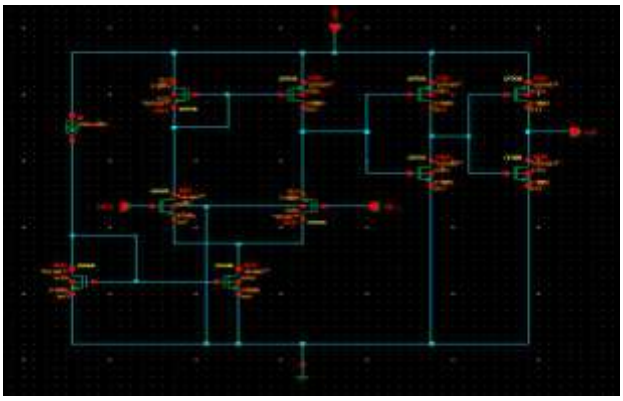

Fig 7: Schematic Diagram of Comparator in 180 nm Technology

The output response of comparator in 90 nm technology and 180 nm technology are shown in Fig. 8 and Fig. 9 respectively. Supply voltage plays an important role in power consumption. As the supply voltage increases, power consumed by the circuit also increases. One of the main parameters of this design is power consumption

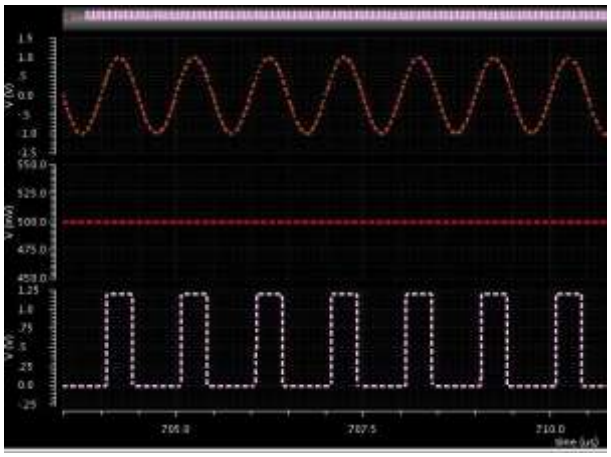

Fig 8: Output Response of Comparator in 90 nm Technology

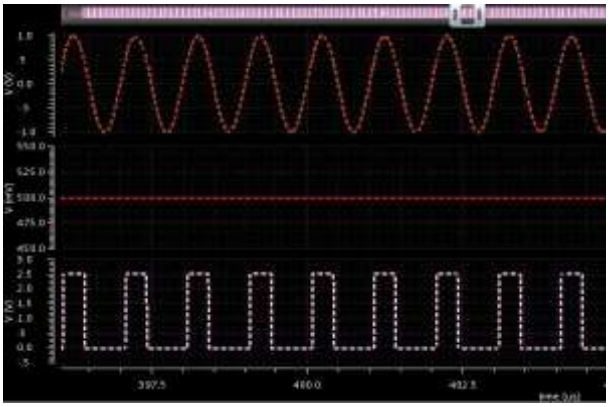

Fig 9: Output Response of Comparator in 180 nm Technology

The power analysis result for 90 nm and 180 nm are shown in Figure. 10, Figure. 11 and Table II. As per Table II, the results of comparator in 180 nm and 90 nm technology are compared. Power consumption is reduced when the technology is scaled from 180 nm to 90 nm technology.

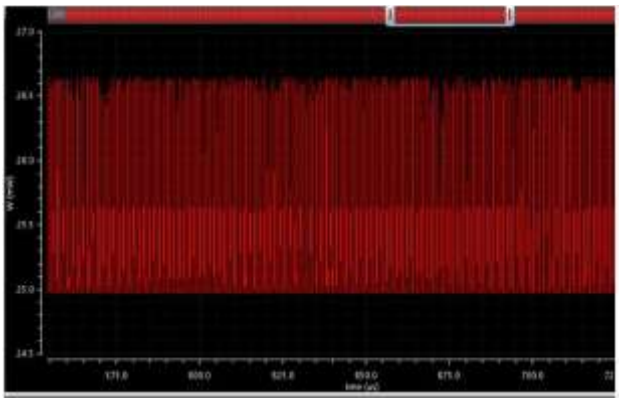

Fig 10: Power Analysis of Comparator in 180 nm Technology

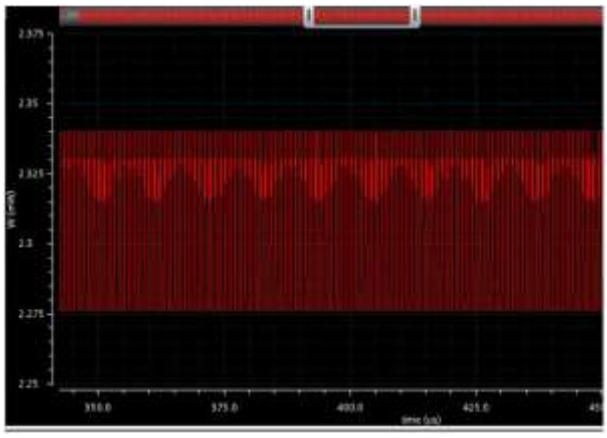

Fig 11: Power Analysis of Comparator in 90 nm Technology

Table 1.Performance Parameters of 1-bit Comparator

Technology	180 nm	90 nm
Supply v voltage(V)	2.5	1.2
Average Power(mW)	25.12	2.29

6. CONCLUSION AND FUTURE WORK

This paper report a CMOS Comparator which is based on the amplifier and inverter. This Comparator can be used for high resolution sigma delta ADCs. The Open loop comparator has been successfully designed and simulated using Cadence Virtuoso tool in 180 nm technology and 90 nm technology. The effect of technology scaling is analysed. The analysis result shows that power consumption in 90 nm technology is 2.29 mW, and that for 180 nm technology is 25.12 mW. By technology scaling a large reduction in the power consumption is achieved. In this paper, open loop comparator is designed. By comparing it with the other comparators like preamplifier latch and others it has more advantages. This comparator is designed for Delta sigma modulator, so , as future work delta sigma modulator is going to be designed using this comparator.

7. REFERENCES

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