Impact of Fin Shape on FINFET Performance

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ABSTRACT
FinFET has been a proven modification of the classical structure of MOSFETs to overcome short channel effect. But the leakage current due to corner effect in trigate FinFET posed impediments in its way. Fin cross section shape of FinFET has considerable impact on leakage performance. In this paper trapezium and inverse trapezium PC FinFETs with various top and bottom width of fin are studied. Results show that rounding the corner and tapering the fin reduce the leakage and improves \( \frac{I_{on}}{I_{off}} \) ratio.

General Terms
FinFET, Leakage

Keywords
PC-FinFET, Corner effect, Multithreshold

1. INTRODUCTION
Miniaturization has been the watchword of the electronics industry [1] for many decades which is achieved by scaling of MOSFETs. It has contributed tremendously to the growth of semiconductor industry and in fact served as the fulcrum of its unimaginable growth in recent years. The shrinkage of the feature size of the device has led to many new challenges and such effects are consummated as short channel effects (SCE) which include \( V_{th} \) roll-off, hot carrier effects, drain induced barrier lowering (DIBL), increase in subthreshold swing and leakage currents, etc. Hence there attained a point where industry has met with a stalemate with bulk devices as it was hardly possible to move further with Moore’s predictions. Power consumption and process variation effects were the important limiting factors of the scaling of conventional transistors beyond 22nm. The Solution to supersede these effects demand performance boosters, like use of novel materials and non-classical device structures to continue further scaling. FinFET transistors have emerged as novel devices having superior controls over short channel effects (SCE) than the conventional MOS transistor devices [2]. FinFETs which provide multithreshold circuits of very low leakage without any area overhead and no requirement of additional mask. However, FinFET exhibit certain undesirable characteristics such as corner effects, quantum effects, tunneling etc. which deteriorates the performance by increasing the leakage current [3]. In Trigate FinFET the premature inversion of the corners occurs due to the charge sharing effect between two adjacent gates. This causes the formation of independent channels with different threshold voltages, explained by the phenomenon corner effect [3] [4]. The mobile carrier density in the corner of trigate FinFET is higher than the other regions and the corner regions are comparable with the planar surface channel region in small dimension devices. A larger part of the current is carried by the corners which can switch on the device. As dimensions are decreasing the effect of corner role on On-state current is increasing and the electron density distributions at the corners are higher compared to the other portion of the channel. In fact, this deteriorates the performance. Rounding the corner has been proposed as one of the ways out and FinFET with round corners is called Partially Cylindrical FinFET (PC-FinFET) [5]. For the same channel length the top fin size for desirable on and off state performance can be optimized with the change in shape of fin from round shape corner to tapered shape fin [6]. In this paper the effect of fin shape on FinFET performance is studied by rounding and tapering the fin. The different PC FinFET structures by various fin top width and various fin bottom width are simulated and compared Threshold voltage, Subthreshold swing, \( \frac{I_{on}}{I_{off}} \) ratio.

2. DEVICE SIMULATION
As the FinFET device structure is complex, 3D device simulation is necessary. So in this work all the FinFET device structures have been simulated using 3D device simulator. All the simulations are done without considering quantum confinement and tunneling. This analysis on the 22-nm bulk FinFET Technology Computer Aided Design (TCAD) model with key geometries given in the Table 1. below. All other model parameters take the default value unless otherwise specified.

| \( L \) | Gate Length | 34nm |
| \( H \) | Height of the Fin | 35nm |
| \( W_{\text{bottom}} \) | Width of the Bottom of the active fin | 15nm |
| \( W_{\text{top}} \) | Width of the top of the active fin | 15nm |
Fig. 1: (a) Trapezium PC FinFET device structure with $W_{\text{top}}=1nm$ and $W_{\text{bottom}}=15nm$ (b) cross section of this device.

Fig. 2: (a) Inverse trapezium PC FinFET device structure with $W_{\text{top}}=15nm$ and $W_{\text{bottom}}=5nm$ (b) cross section of this device.

3. RESULT AND DISCUSSION

All the simulations are done with body doping concentration $1E18$ cm$^{-3}$ and gate work function is 4.6eV for minimizing the leakage. Here all the results are compared with PC FinFET of $W_{\text{top}}=W_{\text{bottom}}=15nm$. First studied the variation of threshold voltage with $W_{\text{top}}$ and $W_{\text{bottom}}$. $V_{th}$ is extracted using the maximum transconductance method with $V_d=0.05$ V. It is observed that threshold voltage increases when $W_{\text{top}}$ of Trapezium ($Tz$) PC FinFET decreases. Threshold voltage is within the range $435mV$ to $472mV$ when $W_{\text{top}}$ varies from $15nm$ to $1nm$ as shown in the Figure 3. And threshold voltage decreases when $W_{\text{bottom}}$ of inverse $Tz$ PC FinFET decreases. Threshold voltage, $V_{th}$, is within the range $435mV$ to $428mV$ when $W_{\text{bottom}}$ varies from $15nm$ to $1nm$ as in the Figure 4.

While observing the Subthreshold swing, SS decreases with decrease in $W_{\text{top}}$. The SS is extracted at a gate voltage ($V_g$) of $0.3$ V. As in the Figure 5, sub threshold swing total range is $10mV/\text{Dec}$ by fin shape variation from rectangular ($W_{\text{top}}=15nm$) to triangular ($w_{\text{top}}=1nm$). Sub threshold swing is less than $92mV/\text{Dec}$. Sub threshold swing also decreases with decrease in $W_{\text{bottom}}$. The total range of SS is $12.8mV/\text{Dec}$ as the $W_{\text{bottom}}$ varies from $15nm$ to $1nm$ as in Figure 6.
Inverse trapezium PC-FinFET structure has more perimeter compared to trapezium PC-FinFET structure with same fin widths. So On current is high in Inverse trapezium PC-FinFET. The leakage current is concentrated in the middle of the fin. In trapezium PC-FinFET leakage current is concentrated in the bottom side so corner leakage current less compared to Rectangular FinFET and Inverse trapezium PC-FinFET. Reducing the top fin width enables leakage reduction. Compared to PC FinFET with $W_{\text{top}}= W_{\text{bottom}}=15\text{nm}$, there is 97.48% reduction in $I_{\text{off}}$ and improved $I_{\text{on}}/I_{\text{off}}$ ratio. The results shown in Figure 7 and Figure 9. The graph in Figure 8 and Figure 10 shows leakage current and $I_{\text{on}}/I_{\text{off}}$ in Inverse trapezium PC-FinFET. The $W_{\text{bottom}}$ variation from 15nm to 3nm provides 95.31% reduction at the cost of 4.7% reduction in saturation current. In triangular FinFET ($W_{\text{top}}=1\text{nm}$) PC FinFET leakage current increases due to tunneling. So Trapezium PC-FinFET gives better leakage performance.

### Table 2. Extracted parameters of trapezoidal PC-FinFETs

<table>
<thead>
<tr>
<th>$W_{\text{top}}$ (nm)</th>
<th>$V_{\text{th}}$ (mV)</th>
<th>SS (mV/Dec)</th>
<th>Leakage current (A/µm)</th>
<th>$I_{\text{on}}/I_{\text{off}}$ ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>472.59</td>
<td>79.37</td>
<td>1.41E-10</td>
<td>2.19E+05</td>
</tr>
<tr>
<td>3</td>
<td>463.82</td>
<td>79.78</td>
<td>1.05E-10</td>
<td>3.07E+05</td>
</tr>
<tr>
<td>5</td>
<td>459.3</td>
<td>80.53</td>
<td>1.64E-10</td>
<td>2.03E+05</td>
</tr>
<tr>
<td>7</td>
<td>453.462</td>
<td>81.607</td>
<td>2.69E-10</td>
<td>1.28E+05</td>
</tr>
</tbody>
</table>
4. CONCLUSION

In this work the impacts of fin shape on FinFET performance in 22nm bulk PC-FinFET are evaluated. Here performance parameters such as threshold voltage, subthreshold swing, leakage current and $I_{on}/I_{off}$ ratio of trapezoidal PC-FinFET and Inverse trapezoid PC-FinFET with different fin width are compared. From the results, it is vivid that Fin shape has considerable impact on leakage performance. Reducing $W_{top}$ results in thinner fin and consume no additional IC area (FinFET foot print is not affected). So fin shaping is the area effective low leakage method. The fin shaping technique can be utilized to generate ultralow leakage FinFETs and multi threshold FinFETs.Compared to rectangular and inverse trapezoid PC-FinFET, inverse trapezoid PC-FinFET gives better leakage control, high $I_{on}/I_{off}$ ratio and threshold voltage range. Hence trapezoid PC-FinFETs shall be proposed as one of the viable choices for Ultra low leakage and Multi threshold applications.

5. REFERENCES

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