Analysis of GAA Tunnel FET using MATLAB

Praveen C S
M.Tech Scholar
Department of ECE
SAINTGITS College of Engineering

Ajith Ravindran
Assistant Professor
Department of ECE
SAINTGITS College of Engineering

Arathy Varghese
M.Tech Scholar
Department of ECE
SAINTGITS College of Engineering

ABSTRACT
In order to improve the energy efficiency of next generation digital systems, transistors with Subthreshold Slope < 45 mV/decade of drain current are needed. Tunnel Field Effect Transistor (TFET) s are attractive new devices for low power applications by its virtues of reduced short channel effects, low off current and their potential for a small subthreshold swing. TFETs ON current (I_{ON}) is usually very low. One solution is a double gate instead of a single gate structure, which will provide I_{ON} improvement. A gate all around (GAA) structure is preferred for further I_{ON} improvement without sacrificing OFF current (I_{OFF}). In order to obtain high I_{ON} and low I_{OFF}, a GAA TFET is modeled with a virtue of meeting the low power and high performance specifications of International Technology Roadmap of Semiconductors (ITRS) projected to year 2020, at a reduced drain voltage(V_{DD}) = 0.5 V.

General Terms
Device Modeling, Emerging Trends in VLSI, Semiconductor Devices.

Keywords
Band to Band Tunneling, Double Gate TFET, Gate All Around Structure, Steep Subthreshold Slope

1. INTRODUCTION
From the early 1970s, the metal–oxide–semiconductor field-effect-transistor (MOSFET) has been the backbone of an ever increasing number of digital integrated circuits. MOSFET device scaling plays an important role in the rapid development of the semiconductor industry. Device scaling allows for more devices and/or functions to be integrated into a single chip with a given silicon area. Gordon Moore, co-founder of Intel cooperation, made an observation in 1965 which is now known as the "Moore's Law". It states that the number of transistors being integrated into ICs will increase exponentially, doubling every 2 years. The number of transistors in a single IC has increased by more than 6 orders of magnitude over the last 40 years. In order to support thevoltage scaling requirement and to reduce the power consumption, new device concepts that can overcome the thermal limit of 60 mV/decade are required.A transistor with a steeper SS allows for transition from ON to the OFF states over a smaller VGS change, keeping the same ION/IOFF current ratio. Such devices are potentially useful in both Low Power (LP) and High Performance (HP) applications. For such systems, we need transistors with Subthreshold Slope (SS) < 45 mV/decade, or lower, on at least three decades of drain current (IDS). Tunneling Field Effect Transistors (TFETs) have garnered interests by its virtues of reduced short-channel effects (SCEs), steep SS and low power consumption [1].

In n-TFETs, carrier injection relies on the band-to-band tunneling (BTBT) of electrons from a degenerate p+ source into the intrinsic channel conduction band, so that high-energy carriers are filtered out by the semiconductor bandgap, thereby achieving steeper subthreshold slopes. For further performance improvement, gate all around (GAA) TFETs are preferred over Double Gate (DG) TFETs. A surround gate structure has more control over the TFET and also will improve ION. GAA TFET is modeled with a virtue of meeting both the low power and high performance specifications of International Technology Roadmap of Semiconductors (ITRS) projected to year 2020, at a reduced V_{DD} = 0.5 V. This paper is organized into 5 chapters. Chapter 2 comprises of the literature review, which introduces the TFET replacement technology for MOSFET. Chapter 3 is the study of GAA TFET. Chapter 4 includes the results and discussions. And finally chapter 5 concludes the paper.

2. MOTIVATION AND LITERATURE REVIEW
In spite of its massive use and monopoly in IC industry, MOSFET have quite a few numbers of limitations. The major limitations of MOSFET include high leakage current, subthreshold slope limitations and tunneling currents [2]. A device with steeper SS would have its I_{DS} modulated over orders of magnitude with a smaller change in V_{GS}. For the same Vdd, a device with a smaller SS would achieve a lower I_{OFF} for a given I_{ON}. Both dynamic power and standby power consumption can thus be reduced. Many FETs whose function is not governed by the drift-diffusion mechanism in the channel region as in the conventional MOSFETS are proposed in order to realize steeper subthreshold characteristics. The intensively studied are steep subthreshold devices are, FinFETs, Impact ionization MOS transistor (I-MOS) [3], Multigate FET (MuGFET), Feedback FET [4], Tunnel FETs etc.

2.1 TFET
Although the principle of band-to-band tunneling was already discovered in 1957 [5] and the first gated p-i-n structure was proposed in 1978, the interest in the first results on TFETs was limited [6]. This changed rapidly after W. Hansch and I. Eisele et al. started to investigate the TFET in 2000 and J. Appenzeller et al. found in 2004 that the TFET might provide a means to overcome the 60 mV/dec switching limit of the classical MOSFET. Following these initial results, several groups started to study the theoretical aspects of TFET operation. TFET structure is similar to MOSFET, but with opposite type doping in Source and Drain. The simplest TFET is a gated P-I-N diode where the source and drain are highly doped with the gate controlling the band-to-band tunneling between the I-channel region and the P+ or N+ region by way of energy band bending in the I-channel region [7]. In order to be consistent with MOSFET technology, the names of the

device terminals are chosen such that voltages are applied in a similar way for Tunnel FET operation. Figure 1 shows an NTFET, the gate induces an N+ channel to form at the surface of the intrinsic channel region in this case and causes a P+/N+ junction to form at the source to channel interface.

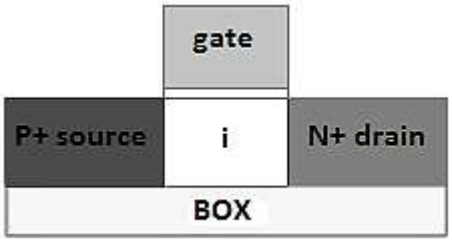

Figure 1: P-i-N TFET structure

2.2 BTBT Theory

BTBT is a quantum phenomenon in which electrons from the valence band (Ev) tunnel through the forbidden energy gap to the conduction band (Ec) with certain tunneling probability (T_{tunnel}), leaving holes in the valence band as shown in Figure 2(a) [8]. Based on Kane's model tunneling current density can be derived as

$$I = \frac{4q}{h}\int T(E)[f_S(E) - f_D(E)]\,dE \quad (1)$$

$$J = \frac{\sqrt{2m^*q^3}\xi V}{4\pi^2\hbar^2\sqrt{E_g}}\; e^{\left(-\frac{4\sqrt{2m^*E_g{}^3}}{3q\hbar\xi}\right)} \quad (2)$$

This design retains the same concept of tunneling and expected to break the 60mV/decade due to carrier transport property which is independent of "KT/q". The potential barrier seen by the tunneling electrons can be approximated as a triangle Figure 2(b), and the tunneling probability T_{tunnel} has an expression as shown in (3) with Wentzel-Kramers-Brillouin (WKB) approximation.

$$T_{tunnel} = e^{-2\int_0^{w_T}\frac{\sqrt{2m_r^*[U(x)-E_c]}}{\hbar}.dx} \approx e^{-\frac{4\sqrt{2m_r^*E_g{}^3}}{3q\hbar\xi}} \quad (3)$$

where w_T is the tunneling width, m_r^* is the reduced tunneling mass, U(x) is the potential energy, ħ is the reduced Planck constant, Eg is the material band gap, and ξ is the uniform electrical field if triangle potential barrier is assumed.

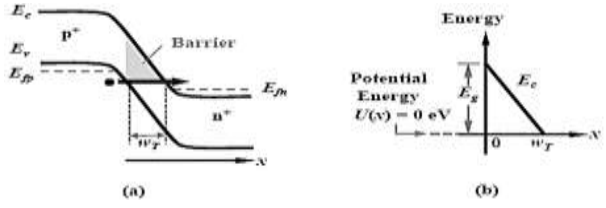

Figure 2: (a) Band diagram of a reverse biased p+/n+ diode (b) The tunneling barrier of the p+/n+ diode in (a) can be approximated by a triangle potential barrier[8]

It should be noted that the smaller w_T , Eg and m_r^* are, the higher T_{tunnel} becomes. For a fixed material, Eg and m_r^* are fixed, and w_T is an indicator of T_{tunnel}. BTBT could occur only if T_{tunnel} is high enough and there are enough electrons at thestarting side under Ev (left side in Figure 2(a)) and enough empty states at the ending side above Ec (right side in Figure. 2(a)).

2.3 Working Principle of TFET

An NTFET is a gated p+ -i- n+ diode, while a PTFET is a gated n+ -i- p+ diode. The gate bias is used to modulate the channel potential of a TFET, and thus to control the BTBT at the interface between the source and the channel as show in Figure 3 (a) and (b). The TFET is switched off at low V_{GS} due to the appearance of a bandgap which cuts off the Fermi tail of carrier concentrations. Therefore, I_{OFF} is very low and limited by the junction leakage which includes both the drift current.

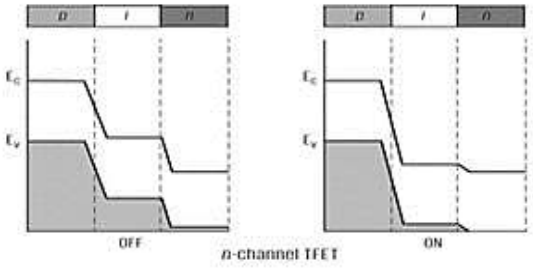

Figure 3: Off-state (a), On-state (b) energy band diagrams of TFET [9]

2.4 Improvement of TFET ON Current

Although some of the reported TFETs achieved SS less than 60 mV/decade, in most of the case, the extremely small SS only appears at very low current level. Therefore, current TFET technology is still far from being a realistic alternative to replace state-of-the-art CMOS for future logic applications. More research efforts are required to further improve the TFET performance, especially the on-state current. In order to achieve a high I_{ON} and a sub-60 mV/decade SS at the same time, some key points need to be considered in TFET realization are junction engineering, gate stack engineering, material engineering and structure engineering. In this paper structure engineering of gate is discussed

3. GATE ALL AROUND TFET

Multigate TFETs will benefit from the additional gates which will provide better control through gate. Enhanced tunneling probability and a boom in I_{ON} are also major advantages of GAA structure.

3.1 Gate Engineering

Gate engineering refers to changing the architecture of the gate terminal of the FET. The parametric variation happening in a multi gate TFET is the variation in screening length, which was actually defined for MOSFET. Screening length, denoted by λ, has several different names like natural length and Debye length, and is referred to as the spatial extent of the electric field, or the length over which an electric charge has an influence before being screened out by the opposite charges around it [10]. It depends upon gate geometry.

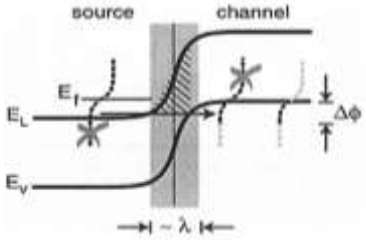

Figure 4: Energy band cross section of Tunnel FET showing λ [11]

Screening length for different gate geometry are given below,

Single gate $\lambda_{SG} = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{si} t_{ox}}$ (4)

Double gate $\lambda_{DG} = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} t_{si} t_{ox}}$ (5)

And for gate all around structure,

$$\lambda_{GAA} = \sqrt{\frac{2\varepsilon_{si} t_{si}^2 \left(1+\frac{2t_{ox}}{t_{si}}\right)+\varepsilon_{ox} t_{si}^2}{16\varepsilon_{ox}}} \quad (6)$$

Where ε_{Si} and t_{Si} are the dielectric permittivity and thickness of the silicon (or semiconductor material used), and ε_{ox} and t_{ox} are the dielectric permittivity and thickness of the gate dielectric.

3.2 Double Gate TFET

When changing from a single-gate design to a double-gate design, TFETs will benefit from the added gate, such that the on-current is boosted significantly, while the off-current, increases by the same factor but remains extremely low in fA or pA range and the device performance does not at all degrades significantly. The main reason behind this is, at low gate bias the tunneling phenomenon takes place at far below the surface and caused low drain current as compared to conventional TFET. However, in high gate bias the tunneling take place at the source-channel junction surface. Hence, for DG TFET the drain current is approximately double because of the presence of both side surfaces compared to its conventional counterpart.When the device body is thin enough, however, the electrostatic control of the tunnel junction by the gate will be improved with a double-gate configuration, and the current will more than double.

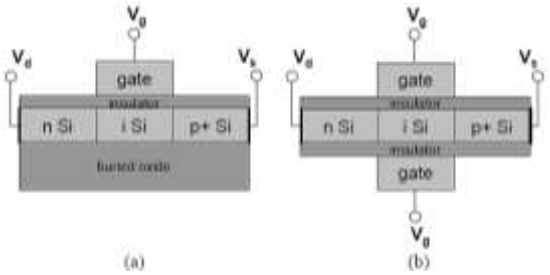

Figure 5: Structure of n-type Tunnel FETs: (a) single-gate and (b) double-gate[12]

3.3 Gate All Around TFET

With the advancements in CMOS applications, GAA transistors are being considered as promising candidate due to excellent gate to channel coupling, highly integrable in circuit functionality and compatibility with existing CMOS technology. Process integration of TFET with GAA structure will increase on-chip devise density and will show good gate controllability. The GAA architecture is an advanced MOSFET geometry where the silicon channel is completely surrounded by metallic gate [13]. Figure 6 shows the progression of device structure form conventional single gated to double gated and to fully GAA device structure. Vertical GAA silicon nanowire platform is already been fabricated by the nanoelectronic group at institute of microelectronics, with its excellent electrostatic control, has shown improved performance compared to planar counterparts [14].

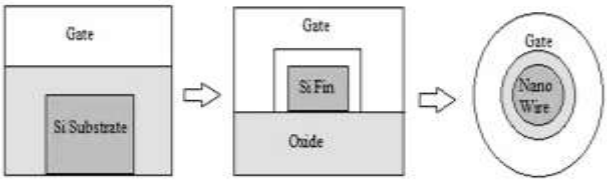

Figure 6: Progression of Device Structure from Conventional Single Gate Planar Device to Fully GAA Structure

Surround gate structure allows more channel width per unit area of silicon, which leads to an increase of the drive current per unit area. Moreover, this structure utilizes a very thin body to eliminate sub-surface leakage path between the source and drain, and thereby provides excellent control of SCEs. Subsequently in future, fully depleted narrow channel with GAA structure are expected promising alternative due to having better gate control, suspension of SCEs, extremely superior short channel immunity with SS < 60mV/decade of I_{ON} and high I_{ON}/I_{OFF} ratio. The excellent device characteristics undoubtedly indicate high potential for further scaling. Generally the body doping of GAA structure TFET is kept lightly doped or undoped which is desirable for immunity against dopant fluctuation effects which give rise to threshold voltage variation.

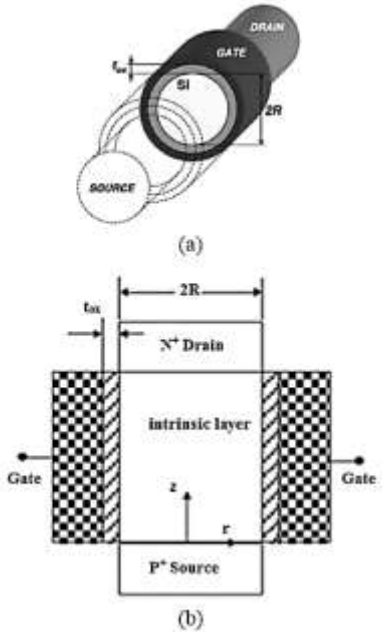

Figure 7: Schematic diagram of Surrounding gate TFET [15]

3.3.1 Impact of GAA Structure on Tunneling Current

The central expression in the TFET model is an experimentally well-established equation for band-to-band, Zener tunneling in planar *p-n* junctions, the primary transport mechanism in tunnel transistors. The two-terminal Zener tunneling behavior is then generalized to three terminals by introducing physics-based expressions for the bias dependent tunneling window $V_{tw}$and a dimensionless factor *f*, which accounts for the superlinear current onset in the output characteristic.

$$I_{dt}(V_{gs}, V_{ds}) = a.f.E.V_{tw}.e^{-b/E} \quad (7)$$

The parameters *a* and *b* are given by,

$$a = \frac{W.T_{CH}.q^3}{8\pi^2\hbar^2}\sqrt{\frac{2m_r^*}{E_g}} \quad (8)$$

$$b = \frac{4\sqrt{2m_r^* E_g^3}}{3q\hbar} \quad (9)$$

Where $m_r^* = (1/m_e^* + 1/m_h^*)^{-1}$ is the reduced effective mass, which is the sum of the reciprocal of the electron, m_e^*, and hole, m_h^*, effective masses. For normalization $m_r^*$is multiplied by the electron rest mass m_0 = 9.11 x 10^{-31}. $E_g$is the semiconductor band gap (1.1eV for Si, 0.35eV for InAs, etc.), $\hbar$ = 1.05 x $10^{-34}$is the reduced Planck's constant, T_{CH} is channel thickness and q = 1.6 x 10^{-19} is elementary charge.

The factor *f* in (7) is given by,

$$f = \frac{1-e^{-\frac{V_{dse}}{\Gamma}}}{1+e^{\frac{(V_{thds}-V_{dse})}{\Gamma}}} \quad (10)$$

Where Γ= 0.06 is the saturation shape parameter

The voltages V_{dse} and V_{thds} are given as,

$$V_{dse} = V_{dsmin}\left[\frac{V_{ds}}{2V_{dsmin}} + \sqrt{\Delta^2 + \left(\frac{V_{ds}}{2V_{dsmin}} - 1\right)^2} - \sqrt{\Delta^2 + 1}\right] (11)$$

$$V_{thds} = \Lambda.\tanh(V_{gs}) \quad (12)$$

Λ = 0.19 is the saturation voltage parameter

Δ is the transition width parameter.

The parameterV_{dse}approaches zero asV_{ds}becomes negative, $V_{dsmin} = 10^{-15}$

The electric field in the tunneling junction is given by,

$$\xi = (\Delta\emptyset + E_g)/\lambda (13)$$

Where $\Delta\emptyset$ – energy range over which tunnelling can take place and λ is the screening length, which varies according to the gate engineering as in (4), (5) and (6)

The tunneling window is given by

$$V_{tw} = \ln\left(1 + e^{(V_{gs}-V_{th})/U}\right) \quad (14)$$

The Urbach factor *U* is considered to be a linear function of gate voltage

$$U = \gamma_0 U_0 + (1 - \gamma_0) U_0 V_{goe}/V_{th} \quad (15)$$

Where V_{goe}also approaches zero as V_{gs}becomes negative,

$$V_{goe} = V_{min}\left[1 + \frac{V_{gs}}{2V_{min}} + \sqrt{\Delta^2 + \left(\frac{V_{gs}}{2V_{min}} - 1\right)^2}\right] (16)$$

V_{min} = 0.0001, γ_0 = 0.5is thetunneling window parameter

$$U_0 = 1.8\ V_t (17)$$

Volt equivalent of temperature V_t is given by,

$$V_t = \frac{k_b(T+273.15)}{q} \quad (18)$$

Where k_b is Boltzmann constant and T is temperature in degree Celsius.

4. RESULTS AND DISCUSSIONS

Relationship between various parameters of TFET like tunneling probability, I_D, V_{GS},V_{DS} etc. are studied and verified by plotting them using MATLAB.

4.1 Tunneling probability variations of SG, DG, GAA TFET

Tunneling probability is plotted against Δϕ for SG, DG and GAA TFETs and the below graph is obtained.

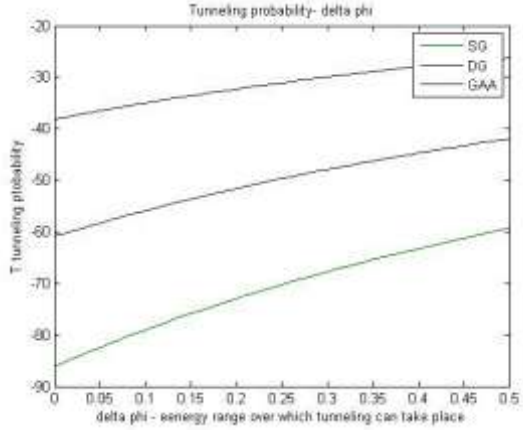

Figure 8: Tunneling Probability of TFET

4.2 I_D-V_{DS} Characteristics of SG TFET

Drain current for the single gate TFET is plotted against drain voltage and its maximum value is found to be around 9 µA for a V_{GS} of .5V.

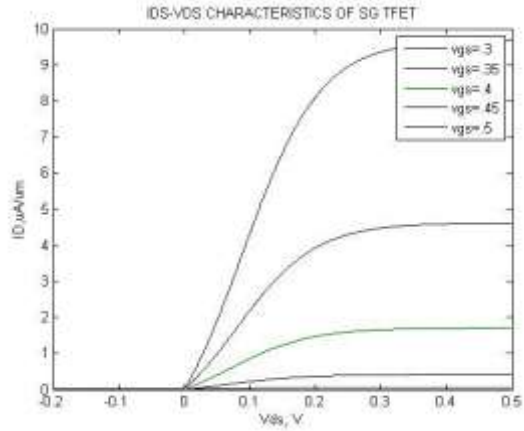

Figure 9: I_D-V_{DS} Characteristics of Single Gate TFET

4.3 I_D-V_{DS} Characteristics of DG TFET

Drain current is plotted against drain voltage and it is found to be almost double that of single gate TFET. Maximum value of I_D is around 20 µA for a V_{GS} of .5V.

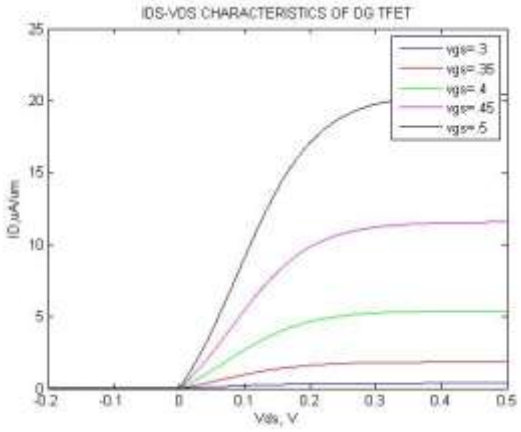

Figure 10: I_D-V_{DS} Characteristics of Double Gate TFET

4.4 I_D-V_{DS} Characteristics of GAA TFET

Drain current for the GAA TFET is plotted against drain voltage and its maximum value is found to be 35µA.

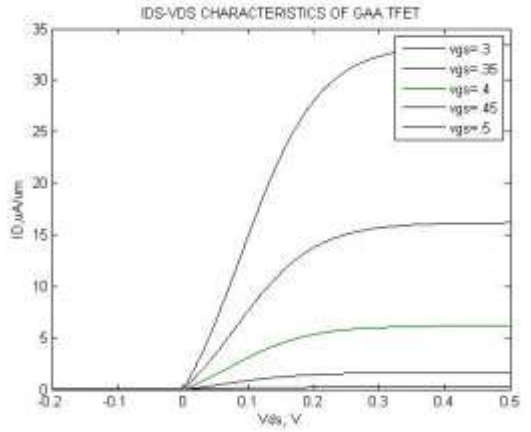

Figure 11: I_D-V_{DS} Characteristics of Gate All Around TFET

4.5 Performance Comparison of TFETS

The performance of the SG, DG, and GAA are compared on the grounds of ON and OFF- current ratios and subthreshold slope. The results are tabulated as shown in table (4.1).

Table 1: Performance Comparison of TFETs

TFET Gate Structure	SG	DG	GAA
$I_{ON\ (max)}$(µA)	9	20	35
I_{OFF}(nA)	5	5	5
I_{ON}/I_{OFF}	$1.8x10^3$	$4x10^3$	$7x10^3$

5. CONCLUSION

The increase in power-dissipation in next-generation electronic circuits must be limited by V_{DD} reduction. For such systems, we need transistors with SS < 45 mV/decade of drain current. TFET is proved to be the number one contender for the throne of CMOS. They garnered interest by its virtues of reduced short-channel effects, steep subthreshold slope, and low power consumption. Even though TFETs have smaller subthreshold slope their I_{ON} is usually very low. One of the possible solutions to improve I_{ON} includes structural changes; a double gate instead of a single gate structure and then to a GAA structure will provide improvement in I_{ON} without sacrificing I_{OFF}. GAA TFET modeled with a virtue of meeting both the low power and high performance specifications of ITRS projected to year 2020, at a reduced VDD=0.5 V is analyzed. GAA TFETs have shown a great deal of performance improvement, compared to single and double gate predecessors. TFET is a field of continuing research; however MATLAB analysis will lead only to limited explorations. Hence detailed studies using advanced TCAD tools are much necessary. A dual material gate variant of the above GAA TFET can yield improved performance, which should be analyzed and optimized.

6. ACKNOWLEDGMENTS

My sincere thanks to Prof. Susan Abe, Head of the Department, Prof. Shajimon K John, PG coordinator, Prof. Dr. K P Zachariah, Asst. Prof. Ajith Ravindran an Er. Ancy P Maniof Department of Electronics and Communication, SAINTGITS College of Engineering, Kottayam Kerala, India

7. REFERENCES

[1] Q. Zhang, W. Zhao, and A. Seabaugh, "Low-subthreshold-swing tunnel transistors," IEEE Electron Device Letters, vol. 27, p. 297, 2006.

[2] S. O. Koswatta, M.S. Lundstrom, and D.E. Nikonov, "Performance Comparison Between p-i-n Tunneling Transistors and Conventional MOSFETs," IEEE Transactions on Electron Devices, vol. 56, pp. 456-465, 2009.

[3] Padilla, C. W. Yeung, C. Shin, C. Hu, and T. Liu "Feedback FET: A Novel Transistor Exhibiting Steep Switching Behavior at Low Bias Voltages" IEDM Tech. Dig., pp. 1, 2008.

[4] K. Gopalakrishnan, P.B. Griffin, and J.D. Plummer, "Impact Ionization MOS (I-MOS) – Part I: Device and. Simulation,", IEEE Trans. Electron Dev., Vol 52, pp 69, 2005.

[5] L. Esaki, "New Phenomenon in Narrow Germanium p - n Junctions", Physical Review, vol. 109, pp. 603-604, 1958.

[6] S. Banerjee, W. Richardson, J. Coleman and A. Chatterjee, "A new three-terminal tunnel device," IEEE Electron Device Letters, vol. 8, pp. 347-349, 1987.

[7] W. M. Reddick and G. A. Amaratunga, "Silicon surface tunnel transistor," Applied Physics Letters, vol. 67, no. 4, pp. 494-496, July 1995.

[8] S. M. Sze and K. K. Ng, Physics of Semiconductor Device, 3rd Edition, John Wiley & Sons, Inc., pp. 422-425, 2007.

[9] Alan Seabaugh, The Tunneling Transistor, IEEE Spectrum, 30 Sep 2013.

[10] J. Knoch, S. Mantl, and J. Appenzeller, "Impact of the dimensionality on the performance of tunneling FETs: Bulk versus one-dimensional devices," Solid-State Electronics, vol. 51, pp. 572-578, 2007.

[11] B. G Streetman and S. Banerjee, Solid State Electronic Devices, 5th edn, New Jersey: Prentice Hall, Inc., 2000.

[12] Verhulst, B. Sorée, D. Leonelli, W. Vandenberghe, and G. Groeseneken, "Modeling the singlegate, double-gate, and gate-all-around tunnel field-effect transistor," J. Appl. Phys., vol. 107, pp. 024518-1-8, 2010.

[13] M.T. Bjoerk, O.Hayden, H.Schmid, H.Riel, and W. Riess, "Vertical surround-gated silicon nanowire impact ionization field-effect transistors" Appl.Phys.Lett., Vol 90, pp 142110, 2007.

[14] N Singh, A Agarwal, L .K Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo N. Balasubramanian and D. L. Kwong, " High performance fully depleted silicon nanowire (diameter < 5nm) gate all around CMOS devices", IEEE Electron Device Lett., vol. 27, no. 5, pp. 383-386, May 2006.

[15] T. S. Arun Samuel, N .B. Balamurugan, T. Niranjana and B. Samyuktha, " Analytical Surface Potential Model with TCAD Simulation Verification for Evaluation of Surrounding Gate TFET", J Electr Eng Technol., Vol. 9, No. 2: 655-661, 2009.