Implementation of High Speed Digital Multipliers using N-MOS based 1-Bit Full Adder

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ABSTRACT
A processor devotes a considerable amount of processing time in performing arithmetic operations. Multiplication is one of the basic arithmetic operations and it requires substantially more hardware resources and processing time than other arithmetic operations. So, Multiplier is one of the most important arithmetic units in processors and also a major source of power dissipation. Reducing the power dissipation, limiting the processing time and transistor count of multipliers are the key factors for designing various digital circuits and systems. To achieve high execution speed, parallel array multipliers are widely used. But these multipliers consume more power. The fundamental units to design a multiplier are adders. Additions are required to be performed using low-power, area-efficient circuits operating at greater speed. This paper aims at analyzing the power dissipation, circuit delay and finally PDP(Power-Delay Product) of parallel array multipliers by using only low power N-MOS based 1-bit full adder. The design has been done using DSCH 2.6c and simulated using 0.18um CMOS technology at 2.5V supply with MICROWIND 2.6a. Comparison of the results of post layout analysis with similar previous multiplier circuits proves efficiency of the proposed multiplier.

General Terms
High speed, Digital Multiplier, NMOS, Full Adder, PDP

Keywords
PDP,C-MOS, N-MOS, Delay, Power, Multiplier, Adder

1. INTRODUCTION
The most important performance parameters of the VLSI systems are power consumption, speed, area and cost. Power consumption must be reduced in a VLSI system for two main reasons. Firstly, reduction of power consumption will lead to increased density of function that can be implemented on a single IC. Secondly, in battery operated systems it is essential to save energy for longer battery life. This reason is very crucial in modern times due to the explosive growth in portable electronic devices like laptops, medical appliances, portable communication systems, multimedia and non-equivalent pace of improvement of battery technology. In general, acceptance of new as well as user friendly applications depends on availability of compact and inexpensive hardware delivering the required high performance. So, design engineers are now concentrating on efficient designs of electronic components to meet the above mentioned critical design issues.

Arithmetic operations are used in all digital electronic systems. Multiplication is one of the complex arithmetic operations. In most of the signal processing algorithms multiplication is a root operation. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip whereas multipliers have large area, consume considerable power and long latency. Traditionally shift and add algorithm has been implemented to design however this is not suitable for VLSI implementation and also from delay point of view. Some of the important algorithm proposed in literature for VLSI implementable fast multiplication is Booth multiplier, array multiplier and Wallace tree multiplier. The fundamental units to design any multiplier are adders. The full adder has been undergoing a considerable improvement. The secret behind this improvement is that the designers always targets on three basic design goals such as minimizing the transistor count, minimizing the power consumption and increasing the speed. In most of the cases, the full adder inevitably forms part of the critical path. So as a whole the full adder performance affects the system performance. In our work a low power N-MOS based 1-bit full adder [15] has been used to design array multiplier and Wallace tree multiplier. The proposed multipliers have been simulated and results of post layout analysis have been compared with similar previous multiplier designs.

The rest of the paper is arranged as follows: Section II mentions the different previously designed full adders along with the circuit of the low power N-MOS based 1-bit full adder to be used for designing multiplier. Section III contains the multiplier circuits chosen for this application. Section IV summarizes the results and analyzes them. Finally, Section IV concludes the paper.

2. ADDER CIRCUIT
Binary addition is the basic and most frequently used arithmetic operation in digital signal processing, image processing, video processing, arithmetic and logic units, floating point processor and microprocessors. Such vast use of this arithmetic operation has created interest among researchers to propose several kinds of designs for the implementation of 1-bit full adder in recent years. Designing low power full adders with improved performance has therefore become a topic of great concern. In recent times, various types of full adders using different logic designs have been proposed. Many full adders circuit are designed using static and dynamic logic style[3],[8]. Among them some designs are Transmission Gate CMOS Adder (TGA) based on transmission gates[2] ,1-bit full adder using low power XOR, XNOR gates, pass transistor and transmission gates[1], Static Energy Recovery Full (SERF) adder[4], Hybrid pass logic (HPSC) full adder[6], hybrid CMOS logic style adder[5] and 8 transistor full adder using 3 transistor XNOR gate[7]. In our work, only NMOS based 1-bit full adder[15] has been used which uses PTL technique for low power. Fig 1 shows the full adder full adder circuit and Table 1 explains its working.

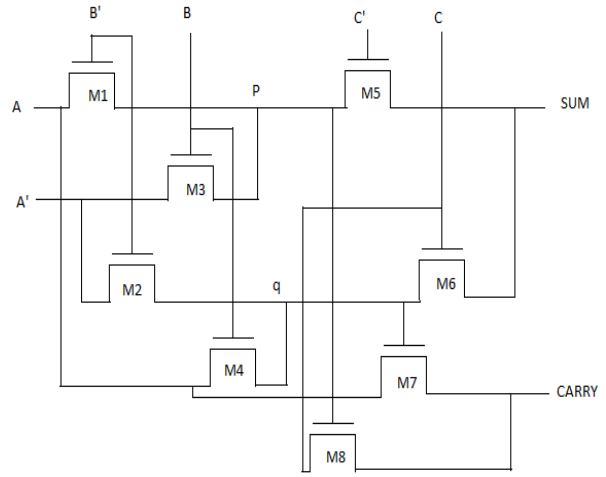

Fig 1: NMOS based 1-bit full adder circuit

Table1. Truth table of the full adder circuit

A	B	C	M 1	M 2	M 3	M 4	M 5	M 6	M 7	M 8	Sum	Carry
0	0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	1	0	0	1	0
0	1	0	0	0	1	0	1	0	0	0	1	0
0	1	1	0	0	1	0	0	0	0	1	0	1
1	0	0	1	0	0	0	1	0	0	0	1	0
1	0	1	1	0	0	0	0	0	0	1	0	1
1	1	0	0	0	0	1	0	0	1	0	0	1
1	1	1	0	0	0	1	0	1	1	0	1	1

3. MULTIPLIER CIRCUIT

With advances in technology, many researchers are trying to design multipliers which offer the following design targets – high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation. Two important algorithm proposed in literature for VLSI implementable fast multiplication is array multiplier and Wallace tree multiplier.

3.1 Array Multipliers

Array multiplier[9],[10],13] is well known due to its regular structure. Multiplier circuit is based on add and shift algorithm. Each partial product is generated by the multiplication of the multiplicand with one multiplier bit. The partial product are shifted according to their bit orders and then added. The addition can be performed with normal carry propagate adder. N-1 adders are required where N is the multiplier length. In the given example, we have 4-bit multiplier and 4-bit multiplicand. By multiplying them 4-rows of partial products can generated as shown in the Fig 2 .The hardware required for the generation of these partial products is AND gates. Using any adder like Carry Save Adder (CSA), Carry Propagate Adder (CPA) we can add the partial products. Fig 3 shows the structure of the array multiplier.

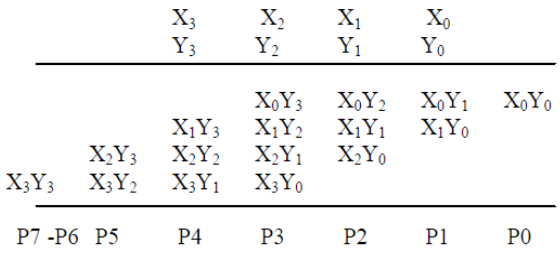

Fig 2: Generation of partial products during multiplication

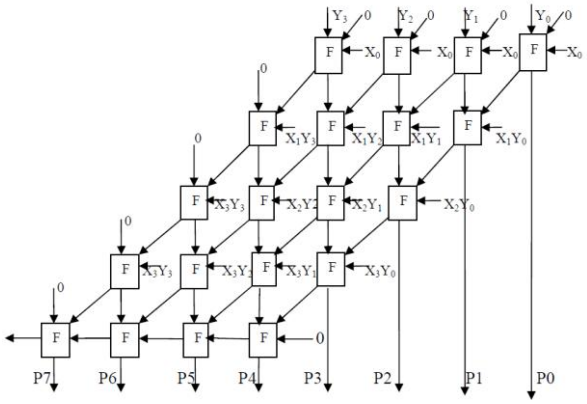

Fig 3: Structure of array multiplier

3.2 Wallace Tree Multipliers

Wallace multiplier[11],[12],[14] implements an aggressive approach to the reduction process where maximum possible reduction is done at every stage. Partial Product matrix rows are grouped into non-overlapping sets of three. Within each three row set, Full Adders reduce columns with three bits and Half Adders reduce columns with two bits. Rows that are not the part of three row set are transferred to the next stage for reduction. This reduction method is applied to each successive stage until only two rows remain. This process is illustrated by 4 bits by 4 bits wallace reduction through diagram shown in Fig 4.

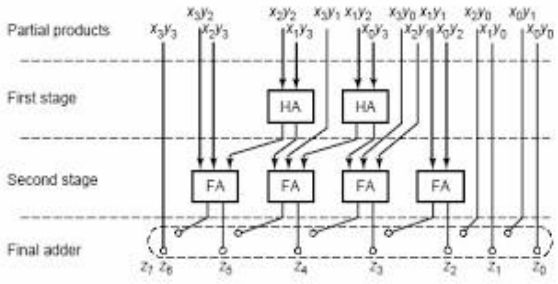

Fig 4: Stages of wallace tree multiplier

Since Wallace Tree is a summation method, it can be used in conjunction with array multiplier of any kind. Fig 5 shows the wallace tree multiplier circuit used in this paper.

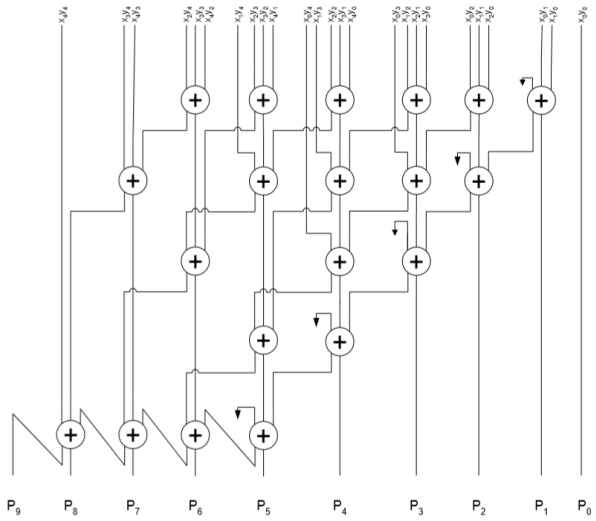

Fig 5: Structure of wallace tree multiplier

4. RESULT AND ANALYSIS

The proposed design has been simulated using 0.18um CMOS technology with DSCH 2.6c at supply voltage of 2.5V and operating frequency of 333 MHz. The layout and post layout simulation has been done using MICROWIND 2.6a with supply voltage 2.5V. All the adder and multiplier circuits have been tested with the same input patterns in the same testing environment.

4.1 Adder Circuit results

Table 2 shows the power dissipation and number of transistors used for various types of full adder circuits. The results are plotted in the Fig 6 which show that the NMOS based adder consumes less power.

Table 2. Comparisons of power consumption and number of required transistors with earlier reported circuits

Sl no	Adder configuration	Power consumption (µW)	No. of Transistors
1	TGA20T	1255.54	20
2	16T adder	591.07	16
3	10T SERF	531.29	10
4	22T hybrid adder	1836.4	22
5	22T HPSC	1533.9	22
6	8T full adder	581.542	08
7	NMOS based full adder	248	14

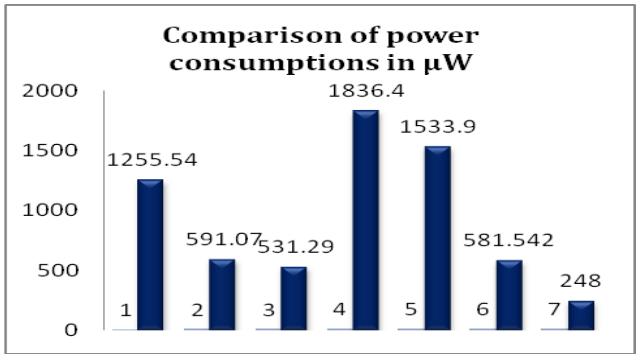

Fig 6: Power dissipation (µW) of different type of full adders

4.2 Array Multiplier Results

Fig 7 shows the simulation result of array multiplier using the N-MOS based 1-bit full adder. The simulation was done using using 0.18um CMOS technology with DSCH 2.6c at supply voltage of 2.5V. Table 3 shows the values of delay, dissipated power and PDP for the array multiplier designed using different type of adders. Fig 8 compares the results of Table 3. From the results it is clear that the proposed multiplier circuit reduces the delay to a great extent but at the cost of increased power dissipation. But the PDP has improved visibly compared to the other circuits. All the readings were taken using MICROWIND 2.6a with supply voltage 2.5V with a load capacitance of 100fF.

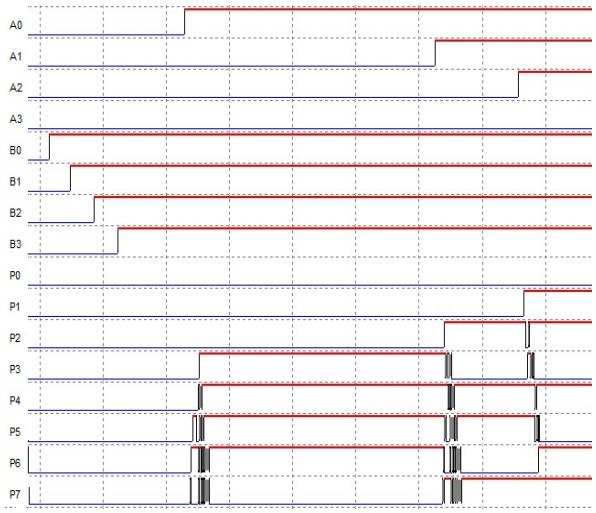

Fig 7: Simulation result of array multiplier

Table 3. Comparisons of delay, power consumption and PDP with earlier reported circuits

Logic style	Delay(ns)	Power(uw)	PDP(fJ)
CMOS	8.3	10.73	89.06
CPL	4.33	24.7	131.82
DPL	4.66	19.72	92.03
Domino	4.05	5.52	22.35
Proposed work	0.15	41	6.15

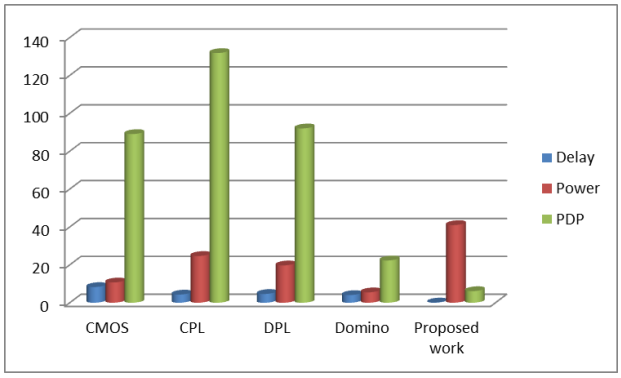

Fig: 8 Comparison of delay, power dissipation and PDP of proposed multiplier with previously reported circuits

4.3 Wallace Tree Multiplier Results

Table 4 lists the values of power dissipation, delay and Power-Delay Product(PDP) of wallace tree multiplier[11] designed using various adder circuits at different supply voltages. Fig 9 shows the comparison of their delays and Fig 10 does the same for their PDP. All the results are tested and gathered using MICROWIND 2.6a with a load capacitance of 100fF.

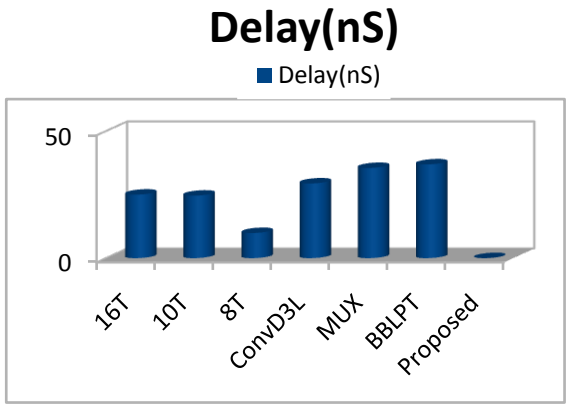

Fig 9: Comparison of delay of proposed multiplier with previously reported circuits

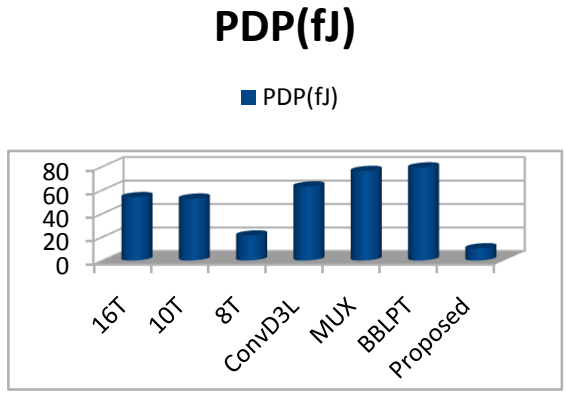

Fig 10: Comparison of PDP of proposed multiplier with previously reported circuits

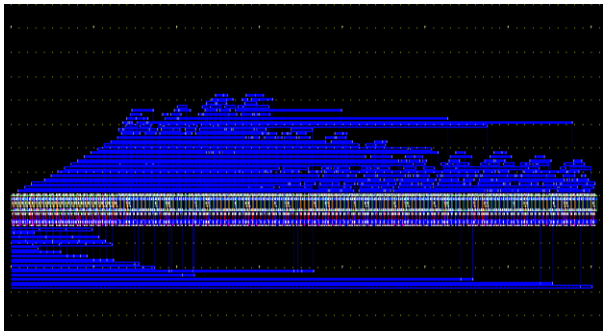

Fig 11: Layout of the design of wallace tree multiplier

Table 4. Comparisons of delay, power consumption and PDP with earlier reported circuits

Specifications of adders for designing multiplier	Power (uW)		Delay(nS)		PDP(fJ)	
	1.5V	2.5V	1.5V	2.5V	1.5V	2.5V
28T	2.14	8.58	44.1	46.8	94.6	402.3
16T	2.14	8.58	25	41.6	53.8	356.8
14T	2.14	8.58	42.4	48.1	90.9	413
10T	2.14	8.99	24.6	37.9	52.6	341.4
8T	2.14	8.56	9.89	37.5	21.2	321
Mirror	2.14	8.58	44.1	48.4	94.7	415.7
TFGA	2.14	8.58	50	59.9	107	514.9
ConvD3L	2.14	8.58	29.4	49.9	62.9	428.2
MUX	2.14	8.58	35.5	37.9	76.1	325
BBLPT	2.14	8.58	36.9	42.7	79.1	366.1
Proposed	514	1880	0.02	0.03	10.28	56.4

The data from Table 4 and comparisons of Fig 9 and 10 again clearly proves the improvement of circuit delay and PDP at the cost of increased power dissipation of wallace tree multiplier due to the use of the previously mentioned full adder. Fig 11 shows the layout of the wallace tree multiplier designed using the N-MOS based 1-bit full adder (PTL logic). The width of the layout is 442µm, and the height is 62µm.

5. CONCLUSION

In this paper performance of only N-MOS based 1-bit full adder has been analyzed first. Then this full adder has been used to design binary multipliers such as array multiplier and wallace tree multiplier and the result of this implementation has been analyzed and compared with the results of previously reported circuits. The proposed multipliers have been simulated using 0.18um CMOS technology with DSCH

2.6c at supply voltage of 2.5V and operating frequency of 333 MHz. The layout and post layout simulation has been done using MICROWIND 2.6a with supply voltage 2.5V. All the adder and multiplier circuits have been tested with the same input patterns in the same testing environment. After analyzing the results it can be concluded that the N-MOS based 1-bit adder can be used effectively to limit the circuit delay of multiplier circuits to a great extent. Reduced delay leads to a improved PDP which is a key factor while designing digital circuits. But this design has a limitation of dissipating high power. This part needs to be considered and treated for further improvement of this design.

6. ACKNOWLEDGMENT

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