# New Architecture of Parallel FIR Filter using Fast FIR Algorithm

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## ABSTRACT

A New parallel FIR Filter structures is proposed based on fast-finite impulse response algorithms, which are beneficial to symmetric coefficients. Parallel (or block) FIR digital filter can be used either for high speed or low- power (with reduced supply voltage) applications. The New parallel FIR structures exploit the inherent nature of symmetric coefficients reducing half the number of multipliers in sub-filter section at the expense of additional adders in pre-processing and post processing blocks. The overhead from additional adders does not increase along the length of the FIR Filter; moreover adders weigh less than multipliers in terms of silicon area. Overall the new parallel FIR structures can lead to significant hardware savings for symmetric convolutions from existing FFA parallel FIR filter especially when the length of the filter is large.The new parallel FIR structures consisting of advantageous polyphase decomposition dealing with symmetric convolutions comparatively better than the existing FFA structures.

## General Terms

Digital Signal Processing(DSP),fast finite impulse response(FIR)algorithm(FFAs), parallel FIR, symmetric convolution,very large scale integration(VLSI)

## 1. INTRODUCTION

Due to the explosive growth of multimedia application, the demand for high-performance and low-power digital signal processing (DSP) is getting higher and higher. Finite-impulse response (FIR) digital filters are one of the most widely used fundamental devices performed in DSP systems, ranging from wireless communications to video and image processing. Some applications need the FIR filter to operate at high frequencies such as video processing, whereas some other applications request high throughput with a low-power circuit such as multiple-input multiple-output (MIMO) systems used in cellular wireless communication. Furthermore, when narrow transition-band characteristics are required, the much higher order in the FIR filter is unavoidable. For example, a 576-tap digital filter is used in a video ghost canceller for broadcast television, which reduces the effect of multipath signal echoes. On the other hand, parallel and pipelining processing are two techniques used in DSP applications, which can both be exploited to reduce the power consumption. Pipelining shortens the critical path by interleaving pipelining latches along the datapath, at the price of increasing the number of latches and the system latency, whereas parallel processing increase the sampling rate by replicating hardware so that multiple inputs can be processed in parallel and multiple outputs are generated at the same time, at the expense of increased area. Both techniques can reduce the power consumption by lowering the supply voltage, where the sampling speed does not increase. In this paper, parallel processing in the digital FIR filter will be discussed. Due to its linear increase in the hardware implementation cost brought by the increase of the block size L, the parallel processing technique loses its advantage in practical implementation. There have been a few papers proposing ways to reduce the complexity of the parallel FIR filter in the past [1]–[9]. In [1]–[4], polyphase decomposition is mainly manipulated, where the small-sized parallel FIR filter structures are derived first and then the larger block-sized ones can be constructed by cascading or iterating small-sized parallel FIR filtering blocks. Fast FIR algorithms (FFAs) introduced in [1]–[3] shows that it can implement a L-parallel filter using approximately (2L-1) subfilter blocks, each of which is of length N/L. FFA structures successfully break the constraint that the hardware implementation cost of a parallel FIR filter has a linear increase along with the block size L. It reduces the required number of multipliers to (2N-N/L) from L x N. In [5]–[9], the fast linear convolution is utilized to develop the small-sized filtering structures and then a long convolution is decomposed into several short convolutions,i.e., larger block-sized filtering structures can be constructed through iterations of the small-sized filtering structures.

However, in both categories of method, when it comes to symmetric convolutions, the symmetry of coefficients has not been taken into consideration for the design of structures yet, which can lead to a significant saving in hardware cost. In this paper, we provide new parallel FIR filter structures based on FFA consisting of advantageous polyphase decompositions, which can reduce amounts of multiplications in the sub filter section by exploiting the inherent nature of the symmetric coefficients, compared to the existing FFA fast parallel FIR filter structure. This paper is organized as follows.

A brief introduction of FFAs is given in Section 2. In Section 3 the Symmetric convolution based FFA structures are presented, in Section 4 Proposed Cascading FFA, in Section 5 Comparisons table is shown, Section 6 gives the conclusion.

## 2. FAST FIR ALGORITHM (FFA)

Consider an N-tap FIR filter which can be expressed in the general form as

$$y(n) = \sum_{i=0}^{N-1} h(i)x(n-i), \quad n=0,1,2,......,\infty \quad (1)$$

where {x(n)} is an infinite-length input sequence and {h(i)} are the length-N FIR filter coefficients. Then, the traditional L-parallel FIR filter can be derived using polyphase decomposition as[3].

$$\sum_{p=0}^{L-1} Yp(z^L)z^{-p} = \sum_{p=0}^{L-1} Xp(z^L)z^{-p} \sum_{r=0}^{L-1} Hr(z^L)z^{-r}$$
(2)

Where

$Xq = \sum_{k=0}^{\left(\frac{N}{L}\right)-1} z^{-k} x(Lk+q), Hr = \sum_{k=0}^{\left(\frac{N}{L}\right)-1} z^{-k} x(Lk + r), Yp = \sum_{k=0}^{\infty} z^{-k} x(Lk+p),$

for p,q,r =0,1,2.....L-1. From this FIR filtering equation, it shows that the traditional FIR filter will require $L^2$ FIR subfilter blocks of length N/L for implementation.

## 2.1 2x2 FFA (L=2)

According to (2), a two-parallel FIR filter can be expressed as

$$Y_0+Z^{-1}Y_1 = (H_0+Z^{-1}H_1)(X_0+Z^{-1}X_1)$$

$$= H_0X_0+Z^{-1}(H_0X_1+H_1X_0)+Z^{-2}H_1X_1 \qquad (3)$$

Implying that

$$Y_0=H_0X_0+Z^{-2}H_1X_1, \qquad (4)$$

$$Y_1=H_0X_1+H_1X_0.$$

Equation (4) shows the traditional two-parallel filter structure, which will require four length-N/2 FIR subfilter blocks, two post processing adders, and totally 2N multipliers and (2N-2) adders. However, (4) can be written as

$$Y_0=H_0X_0+Z^{-2}H_1X_1 \qquad (5)$$

$$Y_1=(H_0+H_1)(X_0+X_1)-H_0X_0-H_1X_1.$$

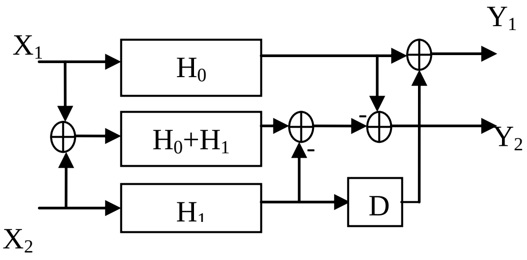

**Fig. 1. Two-parallel FIR filter implementation using FFA.**

The implementation of (5) will require three FIR sub filter blocks of length N/2, one pre-processing and three post processing adders, and3N/2 multipliers and 3(N/2-1)+4 adders, which reduces approximately one fourth over the traditional two-parallel filter hardware cost from (4). The two-parallel (L=2) FIR filter implementation using FFA obtained from (5) is shown in Fig. 1.

## 2.2 3x3 FFA (L=3)

By the similar approach, a three-parallel FIR filter using FFA can be expressed as

$$Y_0=H_0X_0-Z^{-3}H_2X_2+Z^{-3}x[(H_1+H_2)(X_1+X_2)-H_1X_1]$$

$$Y_1=[(H_0+H_1)(X_0+X_1)-H_1X_1]-(H_0X_0-Z^{-3}H_2X_2)$$

$$Y_2=[(H_0+H_1+H_2)(X_0+X_1+X_2)]-[(H_0+H_1)(X_0+X_1)-H_1X_1]-[(H_1+H_2)(X_1+X_2)-H_1X_1] \qquad (6)$$

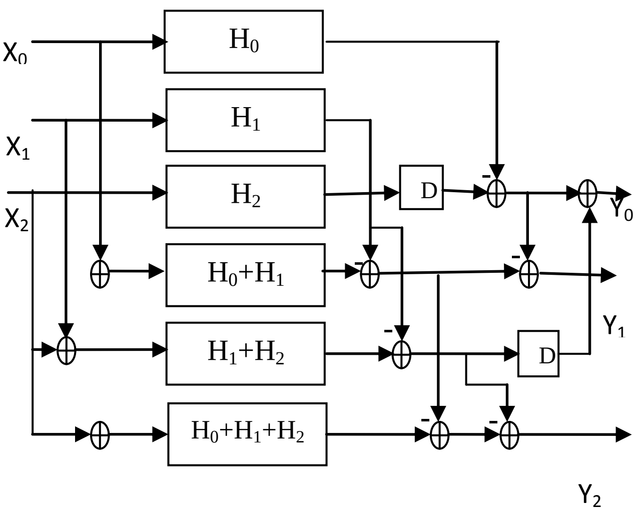

**Fig. 2. Three-parallel FIR filter implementation using FFA.**

The hardware implementation of (6) requires six length-N/3 FIR subfilter blocks, three preprocessing and seven post processing adders, and three N multipliers and 2N+4 adders, which has reduced approximately one third over the traditional three-parallel filter hardware cost. The implementation obtained from (6) is shown in Fig. 2.

## 3. Symmetric convolution based FFA

To utilize the symmetry of coefficients, the main idea behind the proposed structures is actually pretty intuitive, to manipulate the polyphase decomposition to earn as many subfilter blocks as possible which contain symmetric coefficients so that half the number of multiplications in the single subfilter block can be reused for the multiplications of whole taps, which is similar to the fact that a set of symmetric coefficients would only require half the filter length of multiplications in a single FIR filter. Therefore, for an N-tap L-parallel FIR filter the total amount of saved multipliers would be the number of sub filter blocks that contain symmetric coefficients times half the number of multiplications in a single sub filter block (N/2L).

## 3.1 Symmetric convolution based FFA(L=2)

From (4), a two-parallel FIR filter can also be written as

$$Y_0=\{1_{/2}[(H_0+H_1)(X_0+X_1)+(H_0-H_1)(X_0-X_1)]-H_1X_1\}+Z^{-2}H_1X_1,$$

$$Y_1=1_{/2}[(H_0+H_1)(X_0+X_1)-(H_0-H_1)(X_0-X_1)] \qquad (7)$$

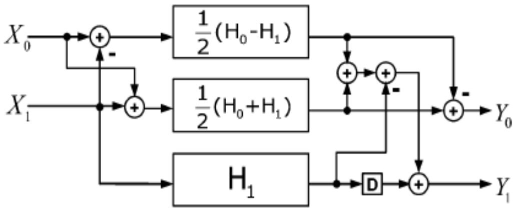

**Fig. 3. Symmetric convolution based FFA two-parallel FIR filter**

When it comes to a set of even symmetric coefficients, (7) can earn one more sub filter block containing symmetric coefficients than (5), the existing FFA parallel FIR filter. Fig. 3 shows implementation of the symmetric convolution two-parallel FIR filter based on (7).

## 3.2 Symmetric convolution based FFA (L=3)

With the similar approach, from (6), a three-parallel FIR filter can also be written as (9). Fig. 4 shows implementation of the proposed three-parallel FIR filter. When the number of symmetric coefficients N is the multiple of 3, the proposed three-parallel FIR filter structure presented in (9) enables four subfilter blocks with symmetric coefficients in total, whereas the existing FFA parallel FIR filter structure has only two ones out of six subfilter blocks. A comparison figure is shown in Fig. 5, where the shadow blocks stand for the subfilter blocks which contain symmetric coefficients. Therefore,foran N-tap three-parallel FIR filter, the symmetric convolution based structure can save N/3 multipliers from the existing FFA structure. However, again, the proposed three-parallel FIR structure also brings an overhead of seven additional adders in preprocessing and postprocessing blocks.

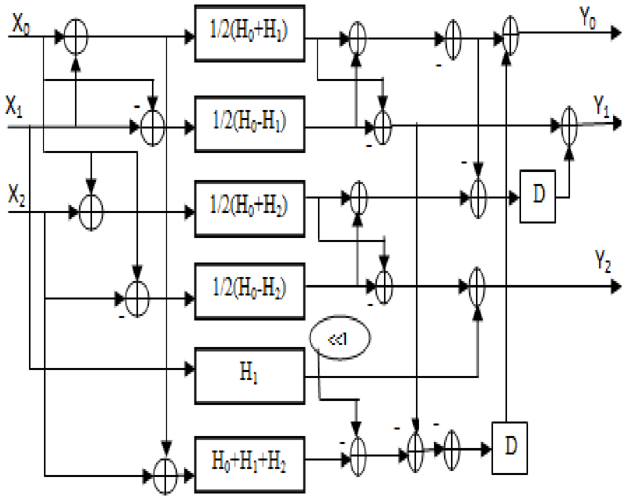

**Fig. 4** ***Symmetric convolution based FFA*** **three-parallel FIR filter implementation**

$Y_0$=1/2[($H_0$+$H_1$)($X_0$+$X_1$)+($H_0$-$H_1$)($X_0$-$X_1$)]-$H_1X_1$+

$Z^{-3}${($H_2$+$H_0$+$H_1$)+($X_0$+$X_1$+$X_2$)-($H_0$+$H_2$)($X_0$+$X_2$)-1/2[($H_0$+$H_1$)($X_0$+$X_1$)-(($H_0$-$H_1$)($X_0$-$X_1$)]-$H_1X_1$}

$Y_1$=1/2[($H_0$+$H_1$)($X_0$+$X_1$)-($H_0$-$H_1$)($X_0$-$X_1$)]+

$Z^{-3}${1/2[($H_0$+$H_2$)($X_0$+$X_2$)+($H_0$-$H_2$)($X_0$-$X_2$)]-1/2[($H_0$+$H_1$)($X_0$+$X_1$)+($H_{0-}H_1$)($X_0$-$X_1$)]+$H_1X_1$}

$Y_2$=1/2[($H_0$+$H_2$)($X_0$+$X_2$)-($H_0$_$H_2$)($X_0$-$X_2$)]+$H_1X_1$ (9)

## 4. Proposed *Cascading FFA*

The proposed cascading process for the larger block-sized proposed parallel FIR filter is similar to that introduced in [1]. However, a small modification is adopted here for lower hardware consumption. As we can see, the proposed parallel FIR structure enables the reuse of multipliers in parts of the sub filter blocks but it also brings more adder cost in pre-processing and post processing blocks. When cascading the proposed FFA parallel FIR structures for larger parallel block factor L, the increase of adders can become larger. Therefore, other than applying the proposed FFA FIR filter structure to all the decomposed sub filter blocks, the existing FFA structures which have more compact operations in pre-processing and post processing blocks are employed for those sub filter blocks that contain no symmetric coefficients, whereas the proposed FIR filter structures are still applied to the rest of sub filter blocks with symmetric coefficients. An illustration of the proposed cascading process for a six-parallel FIR filter (L=6)as an example and the realization is shown in Fig. 5. From Fig. 7, The proposed six-parallel FIR filter will result in 6 more symmetric sub filter blocks, equivalently N/2 multipliers saved for an N-tap FIR filter, than the existing FFA, at the expense of an additional 32 adders. The 6 parallel FIR filter is generated by cascading a (2-by-2) FFA with a (3-by-3) FFA. The process is essentially identical to the process that was used to generate the 4-parallel filtering structure. Beginning with the (2-by-2) FFA is applied resulting in **3** filtering operations. The (3-by-3) FFA is then applied to each of these filters producing the 18 filtering operations that are required in the 6-parallel filtering structure. It should be noted that when (2-by-2) and (3-by-3) FFAs are cascaded, the (2-by-2) FFA is always each of these filters producing the 18 filtering operations that are required in the 6-parallel filtering structure. It should be noted that when (2-by-2) and (3-by-3) FFAs are cascaded, the (2-by-2) FFA is always applied first as this will lead to the lowest implementation cost. The resulting &parallel filtering structure requires 18N/6, or 3N, multipliers and 42 + *18* *(N/6* - 1) adders. This reduced-complexity G-parallel filtering structure provides an area savings of approximately 50% compared to the traditional &parallel filtering structure. The reduced-complexity &parallel FIR filter structure is shown in figure(5).Proposed structure is shown in figure(6).

**3.**

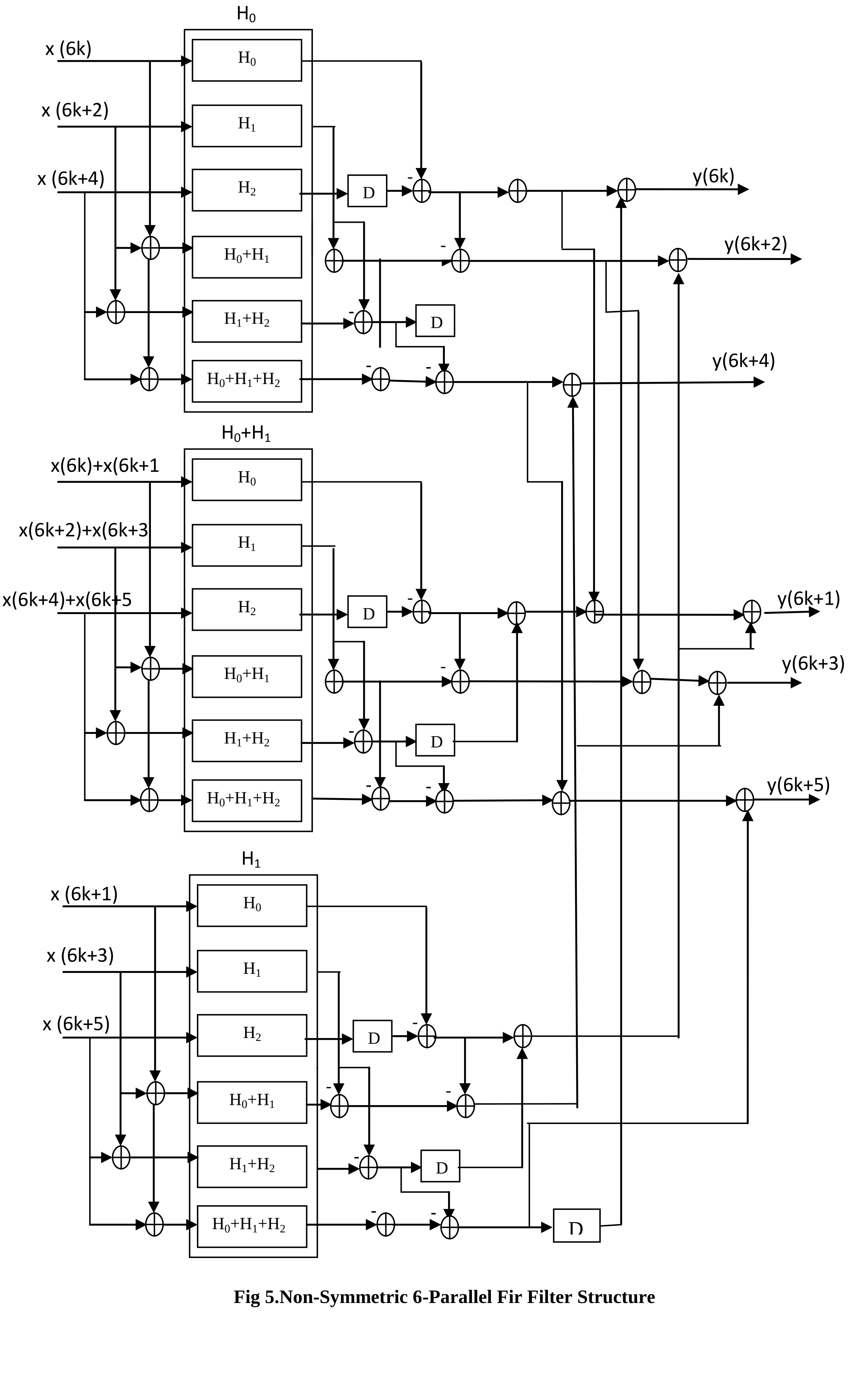

**Fig 5.Non-Symmetric 6-Parallel Fir Filter Structure**

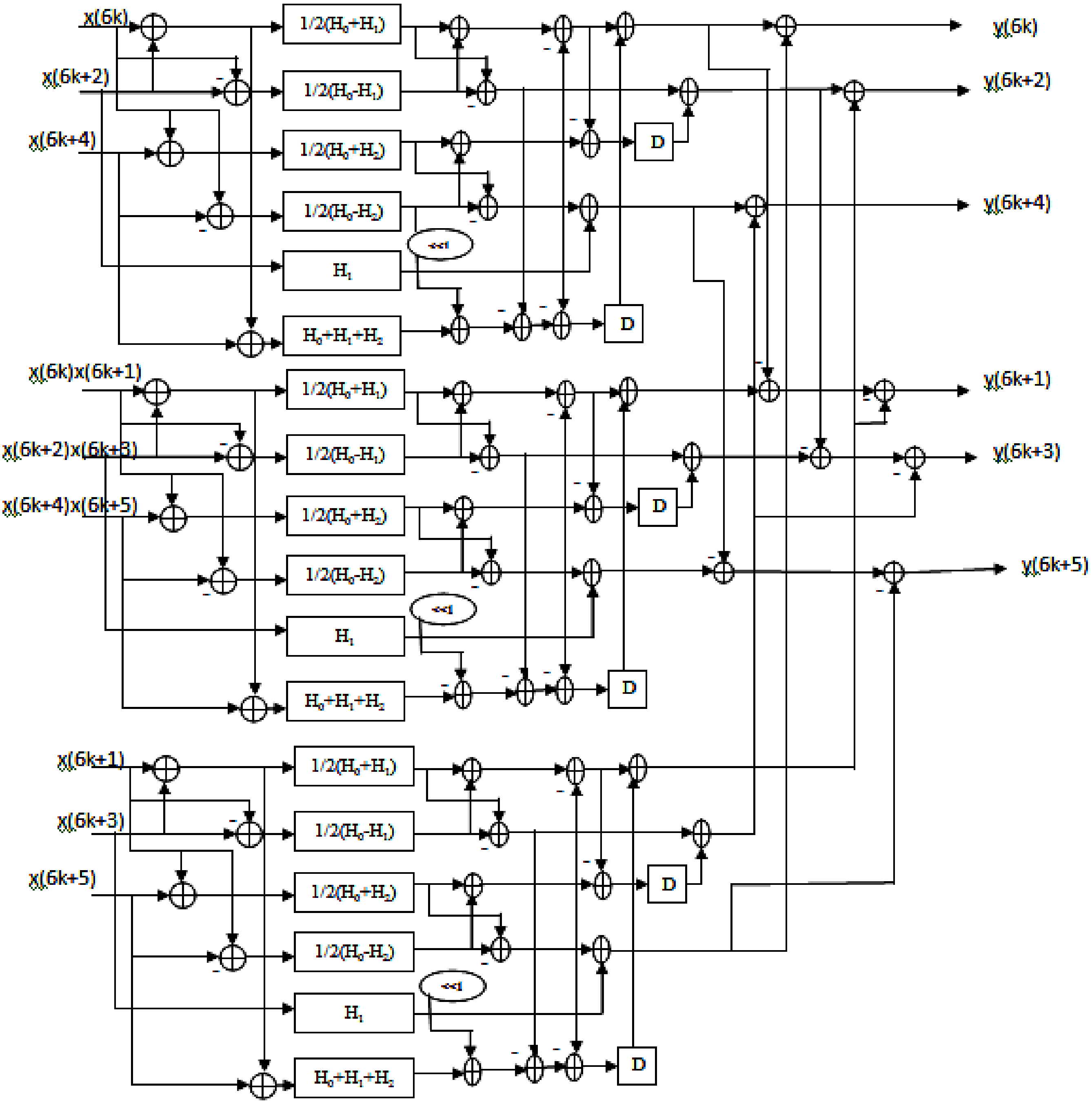

**Fig:6 Symmetric 6-Parallel Fir Filter**

**Table 1:Comparision of AREA**

| | Non-Symmetric 6-Parallel Structure for 24-tap Fir Filter (area utilized) | Symmetric 6-Parallel Structure for 24-tap Fir Filter(area utilized) |
|---|---|---|
| Number of Bonded IOBs | 81% | 81% |
| Total Number of 4 input LUTs | 60% | 51% |
| Number of occupied slices | 65% | 55% |
| Peak Memory Usage | 176 MB | 172 MB |

The ouput obtained is the approximate values, the reduction of area usage will be more as we are increasing the number of tap usage and also by increasing the size of Parallel Fir Filter.

## 5. CONCLUSION

I have presented a new parallel FIR filter structures, which are beneficial to symmetric convolutions when the number of taps is the multiple of 2 or 3. Multipliers are the major portions in hardware consumption for the parallel FIR filter implementation. The proposed new structure exploits the nature of even symmetric coefficients and save a significant amount of multipliers at the expense of additional adders. Since multipliers outweigh adders in hardware cost, it is profitable to exchange multipliers with adders. Moreover, the number of increased adders stays still when the length of FIR filter becomes large, whereas the number of reduced multipliers increases along with the length of FIR filter. Consequently, the larger the length of FIR filters is, the more the proposed structures can save from the existing FFA structures, with respect to the hardware cost. Overall, in this paper, we have provided new parallel FIR structures consisting of advantageous polyphase decompositions dealing with symmetric convolutions comparatively better than the existing FFA structures in terms of hardware consumption.

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