Design of High Speed Dual Modulus Prescaler using Carbon Nanotube Field Effect Transistor

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ABSTRACT

Dual modulus prescaler is one of the main building blocks in Frequency synthesizers. Which gives the flexibility to select channels on the basis of the number of times each of the modulus is selected. Modern frequency synthesizer requires high speed, low power prescaler. This paper proposes the design of such a prescaler using the carbon nanotube based transistor. The two most important performance parameters in the proposed design is speed and power. The biggest limiting factor in this optimization is the technology. The prescaler is often implemented with CMOS technologies. In this paper CNTFET is introduced for designing the high speed and low power 2/3 dual modulus prescaler.

Keywords*:* Dual modulus prescalar, frequency synthesizer, CNTFET, CMOS.

1. INTRODUCTION

With the development of modern communication technology, PLL based frequency synthesizer is continuously improved to meet the increasing demands of wireless systems. For PLL based synthesizer, the integer-N frequency synthesizer is widely used. The dual-modulus prescaler can be used in the feedback to obtain fractional output frequencies. Such synthesizer architectures, called fractional-N frequency synthesizers, allow the reference frequencies to be higher. A dual modulus prescaler is used in high-frequency synthesizer designs to overcome the problem of generating narrowly-spaced frequencies that are nevertheless too high to be passed directly through the feedback loop of the system. The modulus of a prescaler is its frequency divisor. A dual-modulus prescaler has two separate frequency divisors, usually N and N+1 [1]-[3].

Due the scaling limit of the CMOS technology, designing of Prescaler using CMOS technology for the nano applications has limitations. This paper proposes the new design technique, i.e., carbon nanotube based transistor is introduced to design the high speed dual modulus prescalser[4][5]. The rest of this paper is organized as follows: Section II provides the Introduction to dual modulus prescaler. Section III describes the carbon nanotube field effect transistors. Session IV narrates the design of CNTFET based 2/3 prescaler. Session V provide the results and discussion.

2. DUAL MODULUS PRESCALER

Fig (1) shows the block diagram of frequency synthesizer. Frequency synthesizers are crucial components for frequency translation and channel selection in wireless transceivers. Synthesizer design is a challenging task due to the stringent requirements imposed by RF systems. The reference divider can be used to scale highly accurate crystal based input frequencies down to desired levels for the PLL module. The PLL consists of a phase-frequency detector, loop filter and VCO. The operation of the PLL and the programmable counter in the feedback path allow generation of accurate high frequencies from a pure low frequency signal. The programmable P-counter is usually preceded by a prescaler that scales down the high output frequencies A dual-modulus prescaler is a counter whose division ratio can be switched from one value to another by an external control signal. By using the dual-modulus prescaler with an `S' and `P' counter one can still maintain an output resolution specified by the input to the PLL. As long as the S counter has not timed out, the prescaler divides down by N +1. So, both the S and P counters will count down by 1 every time the prescaler counts (N + 1) VCO cycles. This means the S counter will time out after ((N + 1) S) VCO cycles. At this point the prescaler is switched to divide-by-N mode. The P counter still has (P - S) cycles to go before it times out. So after ((P - S) N) more cycles, the system is now reset to the initial condition [6]-[10].

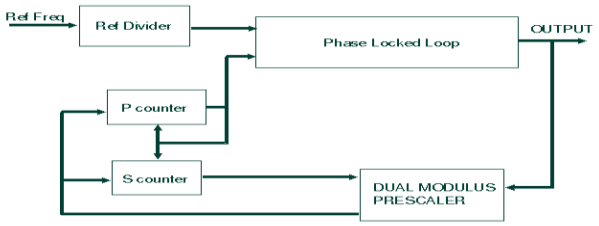

Fig. (1) Frequency Synthesizer.

3. PROPOSED TECHNOLOGY

In CMOS technology the size of the MOSFET is scale down to reduce the size of the device. When the MOSFET scale down to the nanometer ranges, scaling has resulted in increased short-channel effects, reduced gate control, exponentially rising leakage currents, the scaling of MOSFET has progressed rapidly, it may come to an end soon because of the increased short channel effects and power-dissipation constraints. In order to overcome these problems research groups started to explore new devices to replace the CMOS technology. Many new devices has been reported such as single-electron tunneling (SET), rapid single-flux quantum logic, quantum cellular automata (QCA) and carbon nanotube field effect transistor(CNTFET)[11]-[14].

Carbon nanotube field effect transistor (CNTFET) are currently considered, one of the main building block for the replacement of MOSFET based CMOS technology. The core of a CNTFET is carbon nanotube. CNTs are the hollow cylinders. Fig (2) shows the structure of graphene sheet. Carbon nanotubes are formed, when a graphene sheet of a certain size that is wrapped in a certain direction. Fig (3) shows the single walled carbon nanotube (SWCNT). Two atoms in the graphene sheet are chosen, one of which servers the role as origin. The sheet is

rolled until the two atoms coincide. The vector pointing from the first atom towards the other is called the chiral vector and its length is equal to the circumference of the nanotube. Depending on their chiral vector, carbon nanotubes with a small diameter are either semi-conducting or metallic in nature[15]-[17].

Carbon nanotube field effect transistors (CNTFETs) utilize semi conducting single-wall CNTs to assemble electronic devices. A single-wall carbon nanotube (or SWCNT) consists of one cylinder only, and the simple manufacturing process of this device makes it very promising alternative to today's MOSFET.

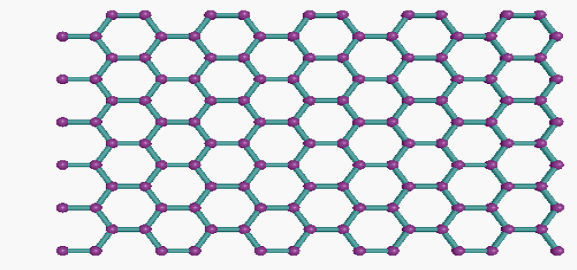

Fig (2) structure of graphene

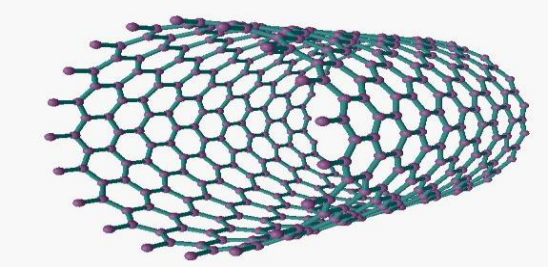

Fig (3) single-walled carbon nanotube

An SWCNT can act as either a conductor or a semiconductor, depending on the angle of the atom arrangement along the tube. This is referred to as the chirality vector and is represented by the integer pair (*n*, *m*). The diameter of the CNT can be calculated based on the following equation (1),

$$D_{CNT} = \frac{\sqrt{3}}{\pi} a_0 \sqrt{n^2 + m^2 + nm} \quad (1)$$

Where a_0 = 0.142 is the inter-atomic distance between each carbon atom and its neighbor. Similar to the MOSFET device, the CNTFET has also four terminals. The current-voltage (I-V) characteristics of the CNTFET are similar to MOSFET's. The threshold voltage is defined as the voltage required to turn on transistor. The threshold voltage of the intrinsic CNT channel can be approximated to the first order, as the half band gap is an inverse function of the diameter and the equation for threshold voltage is given by equation (2).

$$Vth \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{aV_\pi}{eD_{CNT}} \quad (2)$$

Where a = 2.49 Å is the carbon to carbon atom distance, V_π = 3.033eV is the carbon π-π bond energy in the tight bonding model, e is the unit electron charge, and D_{CNT} is the CNT diameter. As D_{CNT} of a (19, 0) CNT is 1.487 nm, the threshold voltage of a CNTFET using (19, 0) CNTs as channels is 0.293V, the device channel consists of a (19, 0), zigzag CNT with a band gap of 0.53 eV and a diameter of 1.5 nm. Fig (4) shows the cross section of a conventional Carbon nanotube field effect transistor (C-CNTFET). The gate dielectric is a 4 nm thick HfO_2 (k = 16) and the device has channel length of 18nm[18]-[25].

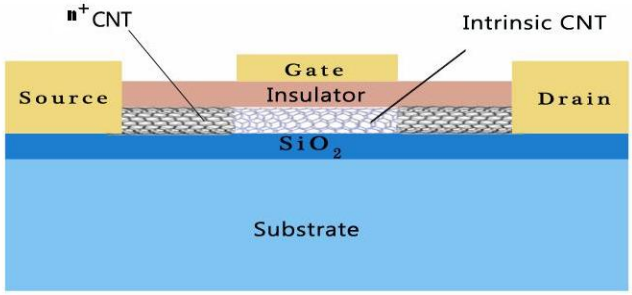

Fig (4) Schematic diagram of a carbon nanotube transistor

The drain to source current of the carbon nanotube field effect transistor is given by equation (3) [26]-[28].

$$I_{DS} = 2\sum_{k_m}^{M}\sum_{k_l}^{L}\left[J_{m,l}\left(0, \Delta\Phi_B\right) - J_{m,l}\left(V_{ch,DS}, \Delta\Phi_B\right)\right] \quad (3)$$

Where M and L are the sub-bands and sub-states respectively. $V_{ch,\,DS}$ is the Fermi level difference with in the channel. $J_{m,\,l}$ is the sub-states current. Fig (5) shows the device current characteristics for both CNTFET and MOSFET. For this simulation carbon nanotube FET gate length is 18nm and MOSFET it is 180nm. CNTFET shows the better performance in terms of high on-state current, high speed and high linearity. Fig (6) shows the NAND gate design using carbon nanotube field effect transistor (CNTFET) and Fig (7) shows the D flip flop design using NAND gates

4. 2/3 DUAL MODULUS PRESCALER

The conventional implementation of any divider/prescaler is using digital counters as shown in fig (8). The division factor that can be easily realized using such logic is of the form 2^N i.e. the

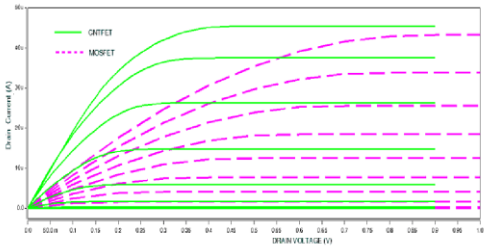

Fig (5) Characteristics of CNTFET and MOSFET

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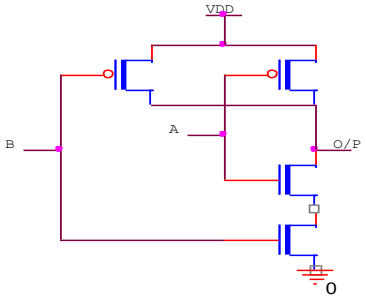

Fig. (6) CNTFET based NAND gate Circuit

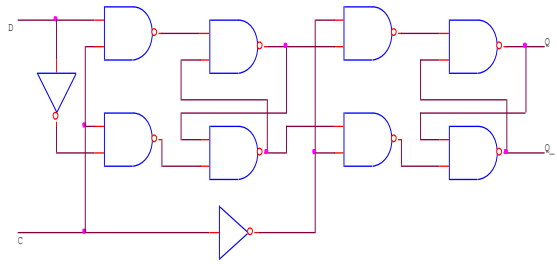

Fig. (7) CNTFET based D Flip Flop circuit

pattern in which the counter counts repeats every 2N cycles. To implement $2^N + 1$, therefore, one extra state of the system needs to be inserted over single pulse duration in the repetitive pattern. Fig shows the simplest 2/3 divider implemented with D Flip Flops and the combinational gate G are inserted in the feedback path of the divider, then the system can be in three states : Q1 Q2 = 01, 10, 11. The Q1 Q2 = 00 is obviously illegal as that implies the previous values of Q2 and G would have had to be in the impossible states of `0' and `1', respectively. In order to control the mod-select an extra gate is required, such as the OR gate in F. This simple 2/3 divider works in divide-by-2 mode when Mod Select is 1 and in divide-by-3 mode for Mod Select 0.

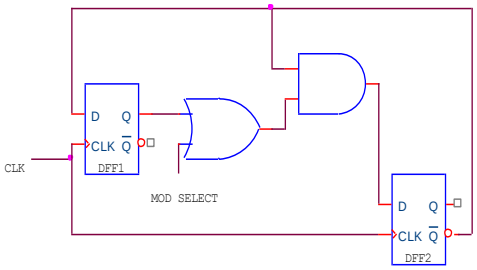

Fig (8) 2/3 Dual-modulus Prescaler

5. SIMULATION RESULTS AND DISCUSSION

A high speed dual modulus prescaler is designed using carbon nano tube field effect transistor in 18 nm technology. The design has been simulated in HSPICE environment. From the simulated results the delay of the proposed design is 25.4p and for CMOS based design 2.56n. For the CMOS based device 0.18µm technology is used with the operating voltage of 1V. Average power consumption of the proposed design is 2.4 µW and CMOS based design is 9.9µW. Power delay product is 60.9aJ for the proposed design. Table 1 shows the parameters of CNTFET and CMOS based technology.

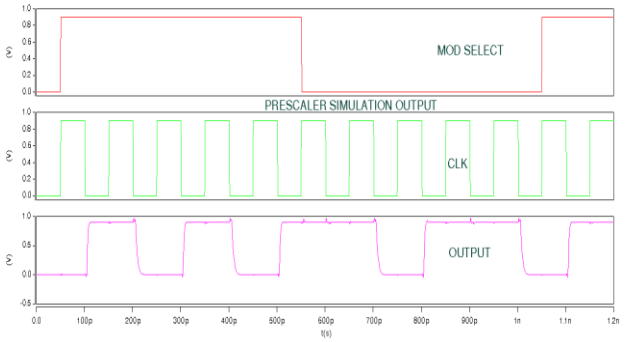

Fig (9) simulation output of 2/3 dual-modulus prescaler

Table. 1 Parameters results of proposed design

PARAMETERS	CMOS	CNFET
Delay(sec)	2.56n	25.4p
Power(watts)	9.9µ	2.4µ
Power Delay Product (joules)	25.3f	60.9a

6. CONCLUSION

In this paper carbon nano tube field effect transistor is introduced for designing the high speed dual modulus prescalar. In this design carbon nanotube used as channel between source and drain, size of the channel has been made in nano metre range. The proposed design gives better performance interms of high speed, low power and low operating voltage. Performance of CNTFET in current conduction is high due their high gate capacitance; this high capacitance value increase ON state current of the device, Gate capacitance value is increased by using high-k dielectric material as gate dielectric. Since the CNTFET requires the less chip area for it's fabrication, the proposed dual modulus prescaler designing technique will be very useful in designing of modern wireless transceivers.

7. REFERENCES

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