An Optimized Circuit of 8:1 Multiplexer Circuit using Reversible Logic Gates

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ABSTRACT
Designing of reversible circuit has become the promising area for researchers. The designing of digital circuits using reversible logic should have zero power loss in ideal conditions. However in practical aspect, it does not occur. This paper illustrates an optimized 8:1 multiplexer circuit grounded on reversible logic using a combination of available reversible logic gates. The multiplexer is optimized on the basis of two parameters namely total number of reversible gates used in the design of the circuits and total garbage outputs generated. This circuit is more advantageous for further designing of any digital circuit with low power loss. The devices designed through this circuit would have better performance as compared to the existing circuits.

General Terms
Low loss digital circuit design.

Keywords
Reversible circuit design, Basic reversible gates, Multiplexer circuit.

1. INTRODUCTION
Field Programmable Gate Arrays (FPGAs) are used to design digital circuit by electrically planning its digital cell connections [1]. Multiplexers show the significant role in the functionalities of FPGAs, therefore designing of a multiplexer circuit using reversible logic would produce low power loss model circuits for FPGAs.

Previously researchers pointed out that digital circuits were prepared with the help of conventional logic gates. These gates were irreversible in nature. Reversible circuit designing is a promising the approach for today in the field of digital circuit designing. In 1961, R. Landauer has revealed that these conventional irreversible circuits drive away some energy owing to the information loss during the operation of the circuit [2]. Later in 1973, Benette has presented that this energy loss can be optimized or even detached from the digital system if the circuits are designed using reversible gates [3].

2. REVERSIBLE LOGIC CIRCUIT DESIGN

2.1 Reversible Logic
Conventionally large number of n:1 gates were being used while designing any circuit. Here n denotes the number of input signals applied and 1 shows the single output produced from the gate. However, in reversible logic gates the input and output signals are represented in the form of n:n. Here both, the number of input signals and the number of output signals are equal. In conventional logic gates, output signals are fewer in number as associated to the number of input signals. On the other hand, in reversible logic gates input and output signals are identical in number. The combinations of output signal at any occasion can offer the exact position of input combinations. This is the foremost reason to name these n:n gates, reversible logic gates[4-6].

2.2 TKS (Reversible) Gate
There are various reversible n:n gates implemented till now[7-13]. TKS gate is a (3,3) reversible gate[14]. Its block diagram is presented in figure 1 and output equations are specified beneath the diagram.

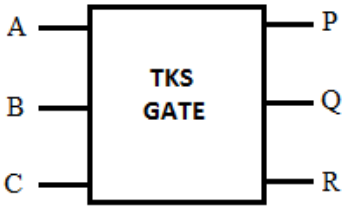

Fig 1: Block diagram of TKS gate

Where –

$P = A.C' + B.C$

$Q = A \oplus B \oplus C$

$R = A.C + B.C'$

In any reversible gate, if we identify the status of output signals (P, Q, R in case of TKS Gate) we can interpret the instance grouping of input stage (A, B, C in case of TKS Gate).

2.3 VSMT (Reversible) Gate
VSMT is a 6:6 reversible logic gate [15]. Which follows the basic characteristics of the reversible logic gates. The block diagram of VSMT gate is presented in figure 2. Here input signals are A, B, C, D, E and F, whereas output signals are P, Q, R, S, T and U.

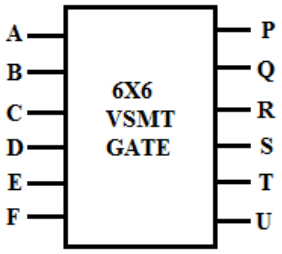

Fig 2: Block diagram of VSMT gate

Output equations of VSMT gate is specified as below-

P = E'.(A.F'+B.F)+E.(C.F'+D.F)

Q = A⊕B⊕C

R = E⊕F

S = C⊕D

T = D⊕E⊕F

U = E

This paper shows the application of VSMT gate and TKS gate to design an optimized reversible circuit for 8:1 multiplexer circuit.

2.4 Multiplexer Circuit

Multiplexer (MUX) is a device which picks any one of the numerous input signals applied and deliver it to the single output line conferring to the arrangement of selection lines applied. Multiplexers are in general used for the translation of parallel data lines into serial one. These are also called Data Selectors, as multiplexer selects one of the given input for the output according to the conditions applied [16]. Figure 3 gives the block diagram of a general 2n:1 multiplexer. Here 2n denotes to the total number of input signal lines and 1 refers to the single output signal line. Total number of selection lines used in multiplexer is n as presented in the figure 3.

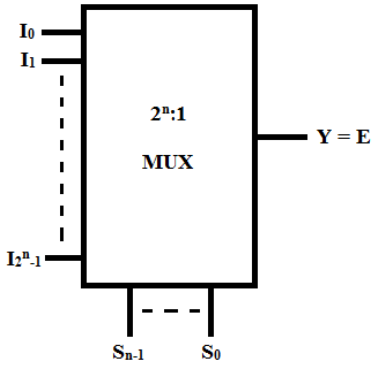

Fig 3: Block diagram of a 2^n:1 Multiplexer

Where output equation is-

$Y = E = I_0.(S_{n-1}'.....S_1'.S_0') + I_1.(S_{n-1}'.....S_1'.S_0) +$

$\ldots\ldots\ldots I_2{}^n{}_{-1}.(S_{n-1}.....S_1.S_0)$

Here input signals of the multiplexer are I_0, I_1, I_2, ... I_{2n-1}, selection lines S_0,S_1, ... S_{n-1} and output Y. Truth table of a 2n:1 multiplexer can be presented as in Table 1.

Table 1. Truth Table of a 2n:1 multiplexer

S. No.	Input Section Lines	Output
	S_{n-1} ..... S_1 S_0	Y
1	0 ..... 0 0	I_0
2	0 ..... 0 1	I_1
-	----------	-
-	----------	-
2^n	1 ..... 1 1	$I_2{}^n{}_{-1}$

It is well known that in any multiplexer circuit the output depends upon inputs as well as the combination of selection lines as shown in the table 1 [17]. Multiplexers of different sizes can be planned by varying the quantity of selection lines i.e. n. A multiplexer of size 8:1 is presented below-

2.5 8:1 MUX

8:1 multiplexer encloses 3 selection lines and 8 input lines. Figure 4 displays the block diagram and output equation of an 8:1 multiplexer [18].

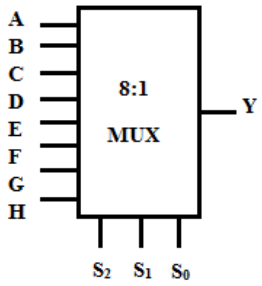

Fig 4: Block diagram of a 8:1 Multiplexer

Output equation of this 8:1 multiplexer can be given as-

$Y = A.S_2'.S_1'.S_0' + B.S_2'.S_1'.S_0 + C.S_2'.S_1.S_0' + D.S_2'.S_1.S_0 + H.S_2.S_1.S_0$

Here we are using S2 as most significant bit (MSB) among the three selection lines are used and S0 as least significant bit (LSB).

3. MULTIPLEXER DESIGN USING REVERSIBLE LOGIC GATES

Multiplexers are considered as mainly data selector circuits. To propose a multiplexer circuit by means of reversible logic gates a small number of conditions for reversible circuit designing has to be followed-

(a) No feedback in the circuit.

(b) Minimum garbage outputs should be generated from the circuit.

(c) Minimum number of reversible logic gates should be used to design the circuit.

Keeping these conditions, any digital circuit using reversible logic can be planned based on the best possible selection of basic reversible gate for minimizing the said variants [19-21].

4. PROPOSED CIRCUIT FOR 8:1 MULTIPLEXER USING REVERSIBLE GATES

Here, we propose the planning of 8:1 multiplexer circuit using the combination of TKS and VSMT gates to realize an optimized circuit as compared to the existing designs. Designing of 8:1 multiplexer are described in subsequent subsections in detail.

4.1 Design of 8:1 MUX using reversible gates

An 8:1 MUX has 3 selection lines and 8 input lines. The design of this multiplexer in reversible logic requires only one TKS gate and two VSMT gates. Input signals are A, B, C, D, E, F, G and selection lines used are S_2, S_1 and S_0. The output variable is denoted by Y. This design approach is shown in the figure 5 below.

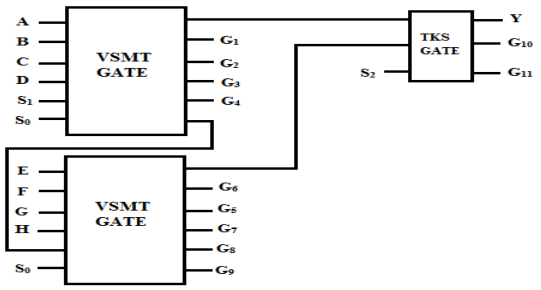

Fig 5: Proposed design of 8:1 MUX using reversible gates

Here all input signals are applied on VSMT gates while output is formulated from the TKS gate. MSB (i.e. S_2) of the selection lines is applied at the inputs of TKS gate whereas rest selection lines are applied to the VSMT gate. This reversible circuit requires a total of three reversible gates for the designing whereas the circuit generates eleven garbage output signals.

5. RESULT AND ANALYSIS

A comparison has made in table 2 between the proposed and existing designs of 8:1 multiplexer in terms of two performance parameters namely total number of reversible gates used in the design and garbage output generated. Table 2 shows that the values of various variants considered for the optimization of the reversible circuit reduces when the circuit for 8:1 multiplexer is designed by using a combination of VSMT and TKS gates.

Table 2: Comparison of various approaches to design a 8:1 Multiplexer using reversible gates

S. No.	Variable	Proposed Design	Existing Design [18]	Improvement
1	Total Number of Reversible Gates used	3	7	57.14%
2	Total Number of Garbage Outputs	11	14	21.43%

These designs are compared on the basis of two parameters namely total number of reversible gates used and total garbage outputs generated. Proposed design uses 3 reversible gates and generates 11 garbage outputs as compared to the 7 reversible gates and 14 garbage outputs in the existing design. Comparison chart for the same is shown in the figure 6 below.

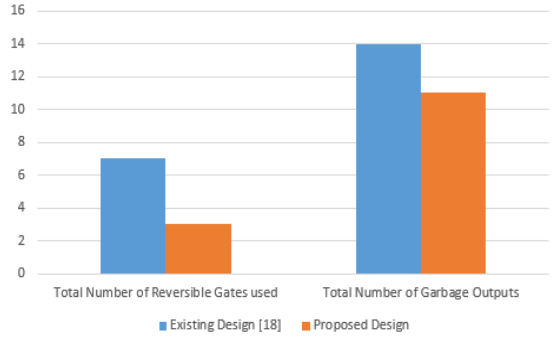

Fig 6: Comparison chart

As shown in the table 2 the proposed design provides 57.14% and 21.43% improvement over the existing design. The proposed circuit is simulated on Modelsim tool and synthesised for Xilinx Spartan-2 with Device 3S50ATQ144 with 200 MHz frequency. The simulation result confirms the proposed reversible logic based circuit is working properly as shown in figure 7.

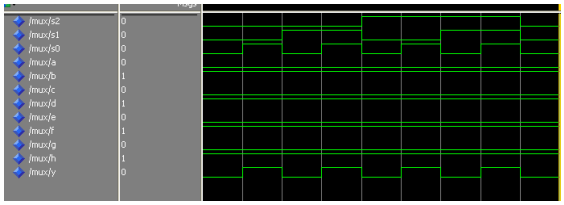

Fig 7: Simulation Result of proposed design for 8:1 multiplexer using Reversible Logic

Simulated circuit of the proposed optimized reversible circuit for 8:1 multiplexer is shown in the figure 8 below.

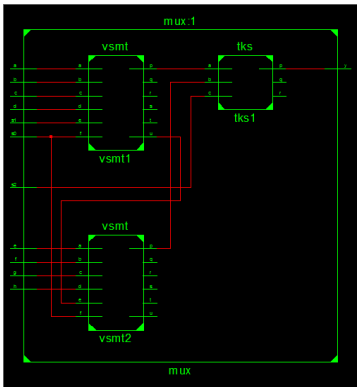

Fig 8: Simulated Circuit of proposed optimized circuit for 8:1 multiplexer using Reversible Logic

6. CONCLUSION AND FUTURE SCOPE

We have designed an optimized circuit for 8:1 multiplexer using reversible logic gates as compared to the existing design for the circuit [18]. The optimized circuit is achieved with help of a combination of TKS and VSMT reversible gates. The proposed circuit for 8:1 multiplexer has better performance as compared to the existing one in terms of total number of reversible gates used in the design as well as total number of garbage outputs generated from the circuit.

This design can be further expanded to accomplish the reversible circuits for numerous functions and devices. Multiplexers are basic constructing blocks of FPGA boards. The proposed multiplexer with reversible gates will support the researchers to employ the FPGAs with reversible gates in low power logical design applications.

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8. REFERENCES

[1] Christian Baumann, "Field Programmable Gate Array (FPGA)", Summary paper for the seminar "Embedded System Architecture", University of Innsbruck, January 13, 2010.

[2] R. Landauer, "Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5, pp. 183- 191, 1961.

[3] C. H. Bennett, "Logical Reversibililty of Computation", IBM J. Research and Development, pp. 525- 532, November 1973.

[4] M.P Frank, "Introduction to Reversible Computing: Motivation, Progress and Challenges", Proceedings of the 2nd Conference on Computing Frontiers, pp. 385–390, 2005.

[5] T. Toffoli, "Reversible Computing", Tech memo MIT/LCS/ TM-151, MIT Lab for Computer Science, 1980.

[6] E. Fredkin and T. Toffoli, "Conservative Logic", Int'l J. Theoretical Physics, Vol. 21, pp. 219- 253, 1982.

[7] H. Thapliyal and N. Ranganathan, "Design of Reversible Sequential Circuits Optimizing Quantum Cost, Delay and Garbage Outputs," ACM Journal of Emerging Technologies in Computing Systems, Vol. 6, No. 4, pp. 14:1–14:35, Dec. 2010.

[8] R. Feynman, "Quantum Mechanical Computers" , Optics News, Vol. 11, pp. 11-20, 1985.

[9] Peres, "Rversible Logic and Quantum Computers", Physical review A, 32:3266-3276, 1985.

[10] D. P. Vasudevan, P.K. Lala , J. Di and J.P Parkerson, "Reversible–Logic Design with Online Testability", IEEE Trans. on Intrumentation and Measurement, Vol. 55, No. 2, pp. 406 -414, April 2006.

[11] P. Kemtopf, "Synthesis of Multipurpose Reversible Logic Gates", Euromicro Symposium on Digital System Design (DSD'02), pp. 259-267, 2002.

[12] H. G. Rangaraju, U. Venugopal, K. N. Muralidhara, K. B. Raja, "Low Power Reversible Parallel Binary Adder/Subtractor", International Journal of VLSI design and communication systems (VLSICS), Vol. 1, No. 3, Sept 2010.

[13] A. N. Nagamani, H. V. Jayashree, H. R. Bhagyalakshmi, "Novel Low Power Comparator Design using Reversible Logic gates", Indian Journal of Computer Science and Engineering (IJCSE), Vol. 2, No. 4 Aug- Sept 2011.

[14] H. Thapliyal, M. B. Srinivas, "Novel Design and Reversible Logic Synthesis of Multiplexer Based Full Adder and Multipliers", IEEE, Vol. 2, pp.1593-1596

[15] Vandana Shukla, O. P. Singh, G. R. Mishra, R. K. Tiwari, "Novel Design of A Multiplexer Circuit Using Reversible Logic", IJCER, Vol. 3, Issue 10, pp. 30-35, Oct 2013.

[16] M. M. Mano (1979), Digital logic and computer design, Prentice-Hall, Inc. (New York).

[17] William I. Fletcher (1980), An engineering approach to digital design, PHI Learning Private Limited, (India).

[18] B. Praveen, S. B. Vinay Kumar, "2n:1 Reversible Multiplexer and its Transistor Implementation", International Journal of Computing Engineering Research (IJCER), Vol. 2, Issue 1, pp. 182-189, Jan-Feb 2012.

[19] B. Raghu kanth, B. Murali Krishna, M. Sridhar, V. G. Santhi Swaroop, "A Distinguish between Reversible and Conventional Logic Gates", International Journal of Engineering Research and Applications (IJERA), Vol. 2, Issue 2, pp. 148-151, Mar-Apr 2012.

[20] H. P. Sinha, Nidhi Syal, "Design of Fault Tolerant Reversible Multiplier", International Journal of Soft Computing and Engineering (IJSCE), Vol. 1, Issue 6, pp. 120-124, January 2012.

[21] D. Krishnaveni, M. Geetha Priya, "A Novel Design of Reversible Universal Shift Register with Reduced Delay and Quantum Cost", Journal of Computing, Vol. 4, Issue 2, pp. 164-173, February 2012.