International Journal of Computer Applications (0975 – 8887)
International Conference on Advancements in Engineering and Technology (ICAET 2017)

Compact Modeling of Tunnel Field Effect Transistor for Ultra-Low Power Design Applications

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ABSTRACT
The IC technology always aims at increasing the package density and the speed. The VLSI technology which is governed by MOSFETs for the past couple of decades. In an attempt to increase the package density the size of the MOSFETS has been scaled down. As the size of the MOSFETs is scaled downwards, sub-threshold leakage current and leakage power in the ICs is increasing. The continued scaling has reached stagnation and further miniaturization of the MOSFET is facing major challenges. The conventional MOSFETs at short channel lengths suffer from high OFF-state leakage currents. They also suffer from numerous other short channel effects. Hence, as an alternative to the MOSFETs, TFETs have been widely studied. TFETs have the asymmetrical source/drain doping profile and they operate as reverse-biased, gated p-i-n tunnel diodes. The on-off switching mechanism in TFETs can be achieved by the gate-voltage induced band-to-band tunneling (BTBT) at the source-channel tunnel junction only. Where as in conventional MOSFETs, only the carriers with energy exceeding the source-channel thermal barrier will contribute the on-state current. TFETs are promising candidates for low power CMOS applications. Modelling the effects of non-idealities on the drain current of a TFET is also an important aspect. High on-state current (Ion), high on-off ratio and steep SS are the critical aspects in TFET design. In, this paper the silvaco TCAD simulation results for both conventional MOSFET & SOI Tunnel field effect transistor and its structure are shown.

Keywords
band-to-band tunnelling, inversion mode, subthreshold swing, ultra-low power design.

1. INTRODUCTION
An essential area of focus in semiconductor technology, and devices in particular, is the continuous scaling down of the device dimensions. We have come a long way in this pursuit – from gigantic vacuum tubes that led to computers the size of large rooms, to the first MOSFET with a gate length of 300 μm, to transistors with gate lengths of 14 nm or less [15]. This has led to integrated circuits containing billions of transistors. Scaling the length of a MOSFET has many benefits, besides the increased number of transistors in a chip. A reduced gate length leads to a reduced gate capacitance, Thereby increasing the switching speed of the circuit. Moreover, the voltage scaling that is a necessary part of device miniaturisation also causes reduction in the power consumption of the device. As the down scaling of conventional CMOS technology results in, rapidly approaching fundamental limits [1, 3]. Alternative device structures are constantly proposed to substitute the traditional

CMOS type devices. That type of device is a gated reverse-biased p-i-n structure, commonly refer to as Tunnel Field-Effect Transistor (TFET). This device is particularly promising for ultra-low-power applications [3]. The most prominent feature of TFETs is their capacity for producing an inverse sub-threshold swing (SS) smaller than the 60 mV/decade thermal limit (at 300 K) of conventional inversion mode MOSFETs [1, 2, 5&4]. Sub-thermal SS is achievable because, the drain current in TFETs is produced by carrier injection from source to channel which is predominantly governed by quantum mechanical band-to-band tunnelling (BTBT) [5], rather than by diffusion as in MOSFETs. Tunnelling is a quantum phenomenon, in which a particle is able to cross a potential barrier even though it does not have the energy to overcome this barrier. Such behaviour is not observed in the case of classical particles. Therefore, any classical analogy used to explain the phenomenon of quantum mechanical tunnelling would necessarily be inaccurate. Instead of taking such a classical analogy, it would be more fruitful to picture the quantum particle as a wave and form a link between this quantum mechanical behaviour and the behaviour displayed by waves. In semiconductors, two different types of models are used to calculate the current resulting from tunnelling – local and non-local models [5-18]. Non-local models treat tunnelling as a process that occurs in spatial coordinates, where electrons tunnel from one point in space to another. The WKB approximation and Landauer's tunnelling formula that are classified as non-local models. Local models, on the other hand, treat tunnelling as a phenomenon taking place from one energy band to another in the E–k space of the material. Two commonly used local models for calculating the tunnelling rate in semiconductors. Kane's model developed by E.O. Kane in 1959, this is one of the oldest and most widely used models for calculating the band-to-band tunnelling rate in TFET models. Hurkx model was developed by Hurkx in 1992 as a recombination model that included the effects of tunnelling. However, the Hurkx model is also used as a tunnelling model by many device simulators [9]. The advantage of the Hurkx model over Kane's model is the inclusion of effects of trap-assisted tunnelling, and density of states. The trans conductance (gm) to drain current (Id) ratio (TCR, gm/Id) in the sub-threshold region, is known as device efficiency, is the corresponding important for analogy applications, as it portrays the available gain per unit of power dissipation of a FET. Because of their smaller SS, TFETs are capable of TCR values in the sub-threshold region higher than the maximum possible value achievable in conventional inversion mode MOSFETs. Thus, a TFET has the potential for delivering higher gain than a MOSFET for the same power dissipation [7]. Although a variety of TFET models have been proposed [8–15] and continue to be developed, fundamental parameters, such as SS and threshold voltage (VT), are still not properly defined for TFETs as they are for conventional inversion mode MOSFETs. For example, the value of SS in TFETs does not remain constant throughout the sub-threshold region but increases with applied gate voltage. Therefore SS is usually quoted as an average or overall number evaluated over several decades of I_D, from nominally off to nominally on values. Likewise, an unequivocal physical mechanism-based definition of threshold voltage does not exist for TFETs, and its extraction remains a challenging task. Therefore it is not

uncommon to expediently quote the V_T of a TFET as the value of gate voltage (V_G) measured at some predefined value of I_D. In Tunnel FETs, the definition of threshold voltage is completely different and threshold voltage is the voltage at which drain current changes from quasi exponential to linear. By these ambiguities, being able to determine V_T still is a very important task for TFET device assessment and circuit [12-14].

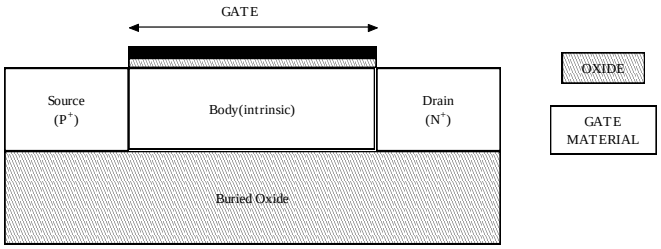
2. WORKING PRINCIPLE OF TFETS

The basic structure of a tunnelling FET. Later, study of many variations of this structure, but the working principle of the TFET is based on this basic arrangement of regions, doping and terminals. Figure 1(a) shows the basic structure of an n-channel TFET. The device has three regions – the source, the channel and the drain. Comparing the structure of an n-channel TFET with that of an n-channel MOSFET, we find that the source doping in a TFET is p-type, whereas it is n-type in the MOSFET. This is the only major difference between a TFET and a MOSFET. The channel region in the TFET is usually intrinsic, or very lightly doped. Now qualitatively examine the behaviour of TFETs. The behaviour of any transistor is usually described by its current characteristics a plot of the current flowing in the device under various biasing conditions. For a transistor, the most significant current characteristics are the transfer characteristics and the output characteristics. These are plots of the drain current in the transistor with respect to the gate and the drain bias, respectively. In this section, we will develop a qualitative understanding of the behaviour of a TFET. The effect of biasing on the drain current of a TFET is best understood by observing the band diagrams of a TFET under various biasing conditions. While studying these, we will qualitatively predict the variation of the drain current with changing bias. Tunnel FETs utilize a MOS gate structure, to control the band-to-band tunnelling process. That is used for a degenerate p-n junction. The schematic energy band diagrams & Cross-section of n- channel TFET in OFF and ON states are shown in Figure 2a and b. The device is generally off state. When 0V is applied to the gate, the conduction band minimum of the channel is above the valence band (V.B) maximum of the source, then band-to-band tunnelling is suppressed [4]. A tunnelling window, qVtw, opens up as the conduction band (C.B) of channel is shifted below the valence band of source. Electrons in the V.B with energy in this tunnelling window tunnel into the empty states in channel and the transistor is ON. The principle of operation for the p-channel TFET with source, channel and drain conductivity types switching is same as in n-channel TFET**.** In the general conventional mode of operation, the n-channel TFET tunnel current is suppressed, when Vgs is low and the tunnel window at the source junction is opened when Vgs positive. However the TFET can turn on at the channel drain junction when the gate bias is sufficiently negative.

As shown in figure 2c, when the gate bias is negative, the V.B maximum of channel can be shifted above the C.B minimum of the drain, leading to electron tunnelling from the channel into the drain. Therefore, the tunnelling window opens up again, with the tunnel junction is shifted from source-channel junction to the drain-channel junction. When this happens the channel conduction changes from one carrier type to another and the transfer characteristic is said to be ambipolar. This behaviour is generally universal across TFET geometries.

When the gate bias is still positive and the drain bias becomes negative, TFET behaves like an Esaki diode, with the signature negative differential resistance (NDR) behaviour appearing in the output characteristics.

N- Channel TFET



P- Channel TFET

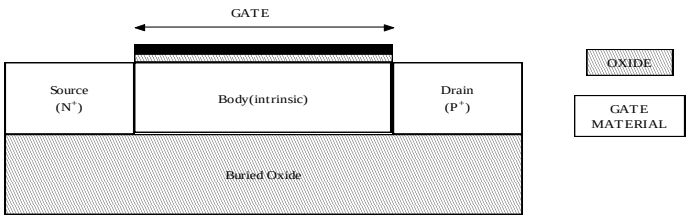


Figure 1. Basic Structure of a TFET

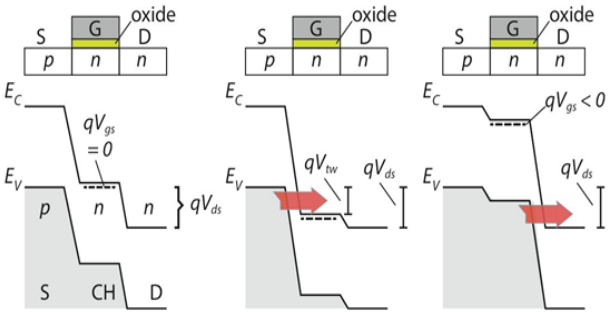


Figure 2. Schematic energy band diagram & Cross-section of an n-channel TFET when the device is biased in (a) OFF (b) ON and (c) ambipolar state where the symbols are defined as follows: EC, conduction band, EV, valence band, V_{gs}, gate-source voltage, V_{ds}, drain-source voltage, and V_{tw}, tunnelling window.

In the quest for transistors that can replace CMOS as the power horse of the semiconductor industry. The steep slope devices such as tunnel field-effect transistors (TFETs) have emerged as the leading contender, because of their capability to keep scaling the supply voltage and lowering the power consumption. TFETs utilize inter band tunnelling as the current conduction mechanism, thus avoiding the Boltzmann-limited subthreshold swing of 60 mV/decade as shown in below figure. From the above figure we can point out the difference between MOSFETs and TFETs. And also the basic structure of TFETs is shown in figure 1. From the basic structure of the TFET we can state that it is like a P-I-N structure (p stands for p-type material, I stands for intrinsic semiconductor and N stands for n-type material).

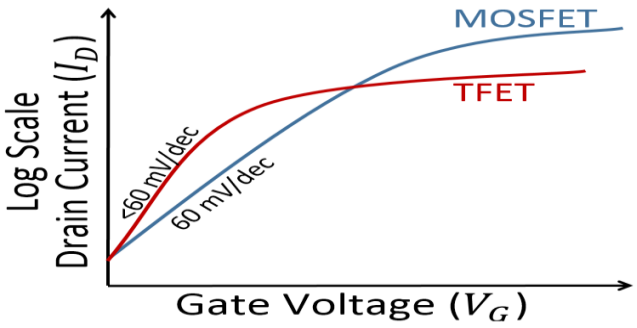


Figure 3: TFET transfer characteristics.

3. SUBTHRESHOLD SWING

The subthreshold swing of a FET is defined as the amount of gate voltage necessary to increase or decrease the subthreshold drain current by a factor of 10, usually expressed in millivolts per decade (mV/dec). An expression is given by the formula below, found in many solid-state device textbooks:

$$SS=\frac{nkT}{q}\ln 10 \qquad \text{Equation 1}$$

Here n is a factor which describes the efficiency of the gate voltage in changing the semiconductor surface potential. Ideally, the surface potential has a value given by a voltage divider consisting of the depletion capacitance (C_D) in series with the oxide capacitance (C_{OX}) equal to 1 + C_D/C_{OX} Due to the thermionic nature of the drain current in a MOSFET, SS is limited by temperature and its minimum possible value is equal to 60 mV/decade at room temperature [4].

4. BAND-TO-BAND TUNNELLING

Tunnelling is a quantum mechanical phenomenon, it occurs due to the wave-like properties of electrons on the atomic scale. When an electron is incident upon an energy barrier, it may be reflected from the barrier or transmitted through. The probability of transmission through, or tunnelling is decided by the height, width, and shape of the barrier. For the case of n-channel TFETs, tunnelling occurs in the source-channel p+n+ junction. At an appropriate gate bias, electrons in the p+ source below the source Fermi level may tunnel through the energy gap into empty states above the Fermi level in the conduction band of the channel [4].

5. RESULTS AND EXPERIMENTAL DATA

The simulation is done by using silvaco TCAD, two MOSFETS models have been modelled and simulated.

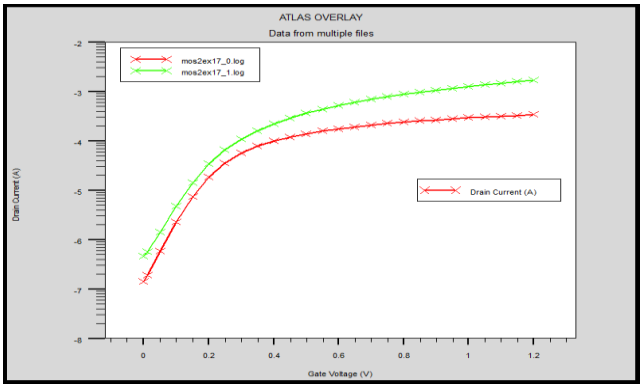


Figure 4: I_d vs V_{gs} characteristics

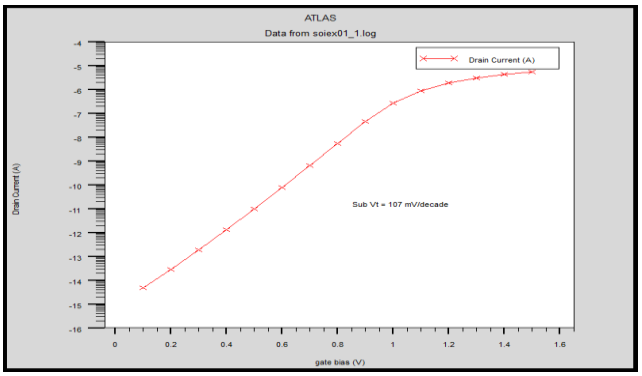


Figure5: Subthreshold slope for conventional NMOSFET

From the figure 4 and 5 it is evident that tunnel fet have Subthreshold Slope (SS) is less than MOSFET that is less than 60 mv/decade.

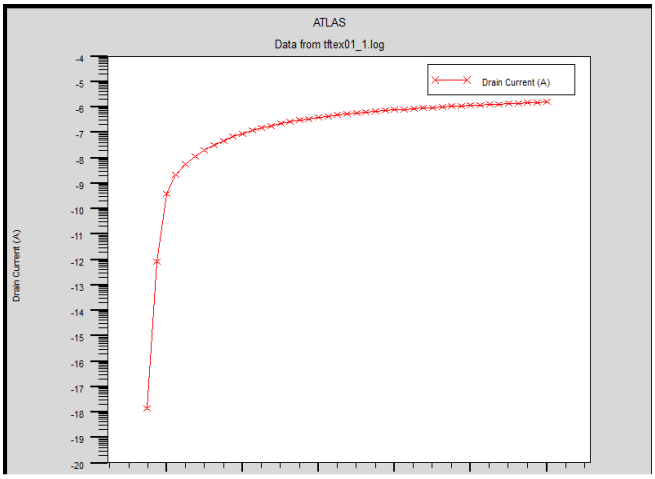


Figure 6: Subthreshold slope for conventional Tunnel FET

Based on the structure, TFETs can be broadly classified into two categories: planar and three-dimensional structures. A planar TFET is a device in which the current-carrying surface is planar. The device can be made on a bulk silicon wafer or on an SOI wafer. For better gate control over the channel, SOI TFETs are preferred over bulk TFETs, High on-state current (Ion), high on-off ratio and steep SS are the critical aspects in TFET design. But it is also involved in scaling of supply voltage (VDD) for power consumption reduction without jeopardizing the performance. More efficient design in TFET prototype demonstration can be made with significant improvement of the tunnelling limited Ion and reduction of SS. The design of TFET involves the tunnelling barrier reduction can be achieved by low band gap materials, hetero-band-alignment, gate electrostatics improvement (e.g. gate-all-around, ultra-thin body & effective oxide thickness (EOT) reduction), and low interface states to suppress the trap-assisted tunnelling (TAT) [14-18].

The simulation of an SOI TFET has a channel length (L) of 200 nm and a gate oxide thickness (T_{ox}) of 2 nm. The thickness of the silicon film (T_{Si}) is 10 nm. The source/drain regions have a doping of $10^{21}/cm^3$ and a length of 50 nm. This is a p-channel TFET and hence the source doping is of n-type and the drain doping is of p-type. The buried oxide thickness is 180 nm. The gate metal wok function is 4.8 eV in order to enhance band-to-band tunnelling at the source channel junction. In a TFET, most of the tunnelling occurs at the

source–channel junction and hence it is necessary to define a finer mesh at this junction. Due to a low ON-state current, there is less variation in physical quantities in the rest of the channel and hence we can afford to have a coarser mesh in the channel. Drain side tunnelling is an important phenomenon in the TFET and hence we should define a finer mesh at the drain–channel junction. In the *y*-direction, the electrostatics is mostly like a MOSFET unless we are defining a vertical tunnelling structure. In this Simulation, we had used Kane's model for the band-to-band tunnelling model, which is a local model used for tunnelling.

Table 1: Device Parameters

Parameters	**Value**
Channel length (L)	200 nm
Gate oxide thickness (T_{ox})	2 nm
Thickness of the silicon film (T_{Si})	10 nm
Source/drain doping	$10^{21}/cm^3$
Source/drain length	50 nm
Buried oxide thickness	180 nm
Gate metal wok function	4.8 eV

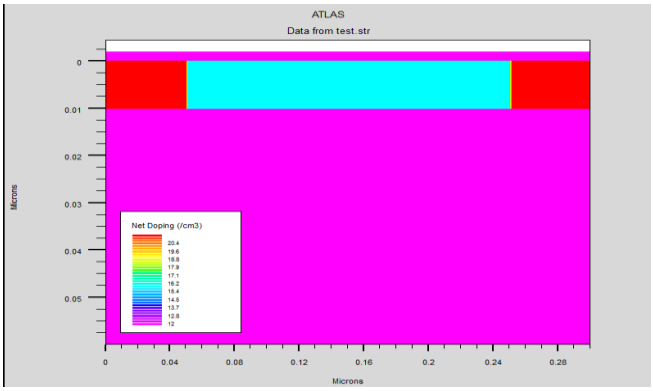


Figure 7: The structure file of the SOI TFET showing the different regions and the doping profile (in log scale) in the device.

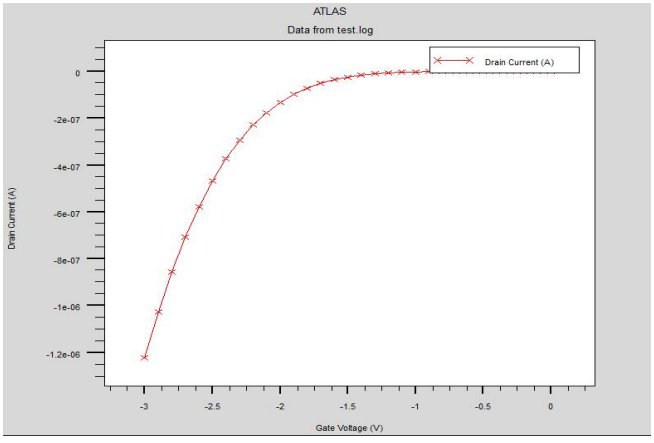


Figure 8: The log file of the SOI TFET showing the drain current (I_D) versus gate voltage (V_{GS}) characteristics.

6. CONCLUSION

TFETs are the most promising steep-slope switch candidate. It have the potential to use a supply voltage significantly below 0.5 V and then offering efficient power dissipation savings. Because of their low off currents, they are ideally suited for both Ultra low-power and low-standby-power logic applications operating at moderate frequencies.

In this paper the subthreshold slope for both conventional MOSFET and Tunnel FETs are shown, it is clear that tunnel FETs is having subthreshold slope less than 60 mv/decade. SOI TFET Simulation, Kane's model is used to find the generation rate of the carriers due to band-to-band tunnelling.

In future Tunnel FETs are simulated with HETRO structure and vertical tunnel FETs are to be analysed.

Hence Tunnel FETs are suitable for Ultra-Low Power Applications.

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