An Ultra Low Power Fast Locking CMOS Phase Locked Loop for Wireless Communication

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ABSTRACT
In this paper fast locking CMOS phase locked loop is proposed. It is designed using Cadence virtuoso gpdk 45nm CMOS technology. It is used 1 volt power supply for operation of the circuit. This proposed circuit will be very useful in clock generation in microprocessor, frequency synthesizer for cell phone, fast locking in digital aid circuits.

Keywords
Phase Locked Loop (PLL), Phase Detector (PD), Charge Pump, Voltage Controlled Oscillator (VCO), Loop Filter, Frequency Divider.

1. INTRODUCTION
A PLL is feedback system that compares the output phase with the input phase. The comparison is performed by a "phase comparator" or "phase detector" (PD). It is a circuit whose output V_{out} is linearly proportional to the phase difference $\Delta\Phi$. In general relation between V_{out} and $\Delta\Phi$ is linear, crossing the origin for $\Delta\Phi$ =0 is called gain of the phase detector, the slope of the line K_{PD} is expressed in V/rad. [1] which is shown in Fig 1.

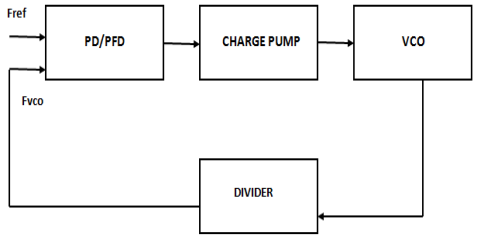

Fig. 1 Conventional PLL

A conventional PLL consists of a Phase Frequency Detector (PFD), Loop Filter (LPF), Voltage Controlled Oscillator (VCO), and Divider. The PLL model is designed to manage a trade-off between the PLL bandwidth and the locking time [2].

2. METHODOLOGY
XOR gate is the best example of phase detector which is shown in Fig. 2. In this figure it is expressed that the phase difference between the inputs varies, so does the width of the output pulses. While the XOR circuit produces error pulses on both rising and falling edges [1]. The phase detector is the core element of a phase locked loop, PLL. Its works enables the phase differences in the loop to be detected and the resultant error voltage to be produced.

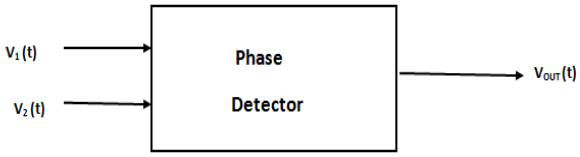

Fig. 2 Block diagram of Phase Detector

Here, schematic diagram of phase detector is shown in Fig.3. It is consist with four 2-input CMOS NAND gate. Gate are connected with two inputs A and B and output Y and its transient responses are determined at various phases which are shown in Fig.4 at phase difference at 0^0, in Fig.5 at phase difference at 90^0 , in Fig.6 at phase difference at 180^0 and in Fig.7 at phase difference at 270^0 respectively.

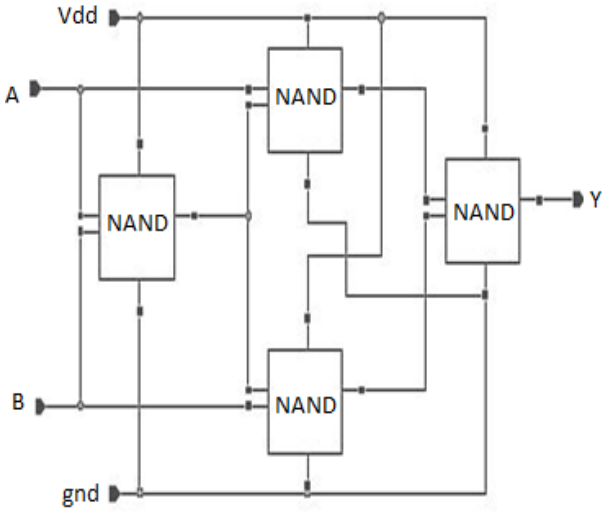

Fig.3 Schematic diagram of Phase Detector

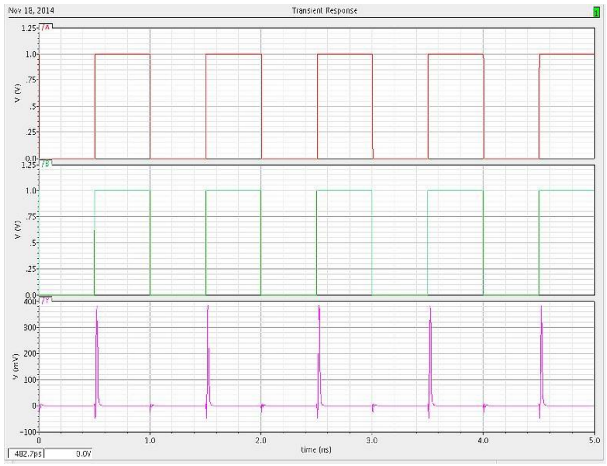

Fig. 4 Transient response at $\Delta\Phi \approx 0$

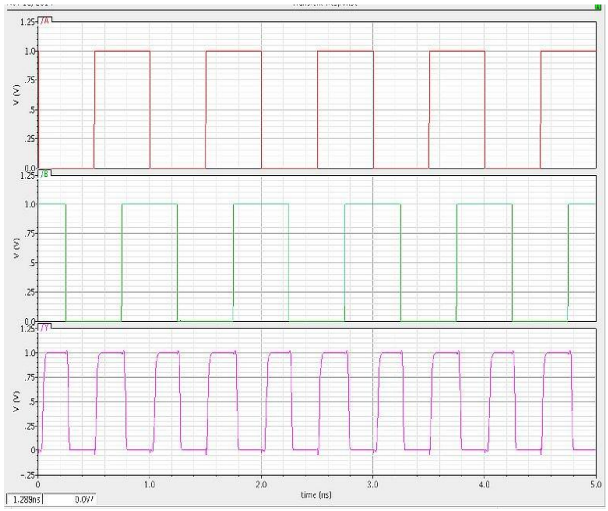

Fig. 5 Transient response at $\Delta\Phi \approx \Pi/2$

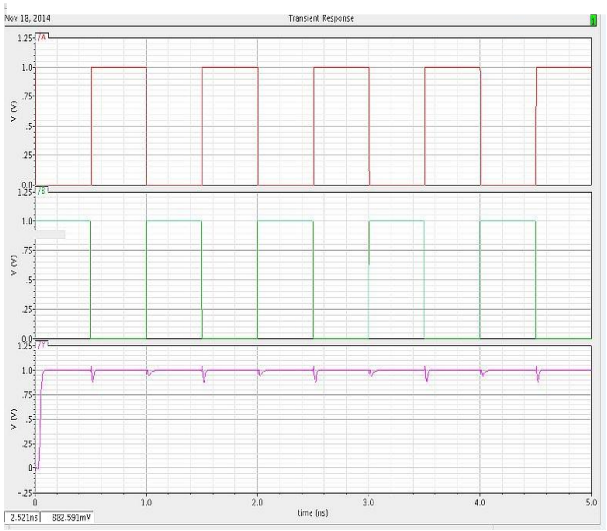

Fig. 6 Transient response at $\Delta\Phi \approx \Pi$

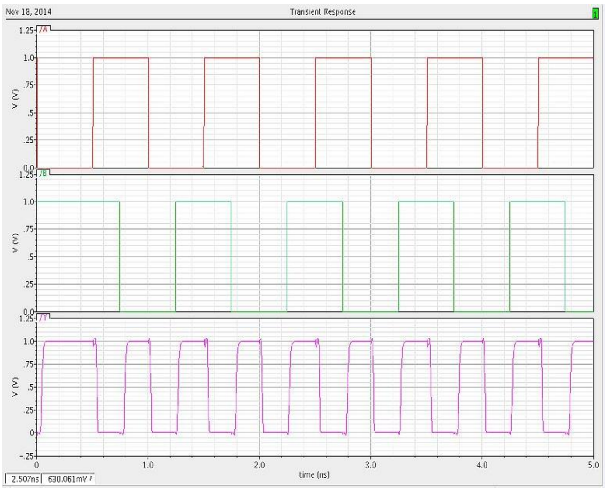

Fig. 7 Transient response at $\Delta\Phi \approx 2\Pi$

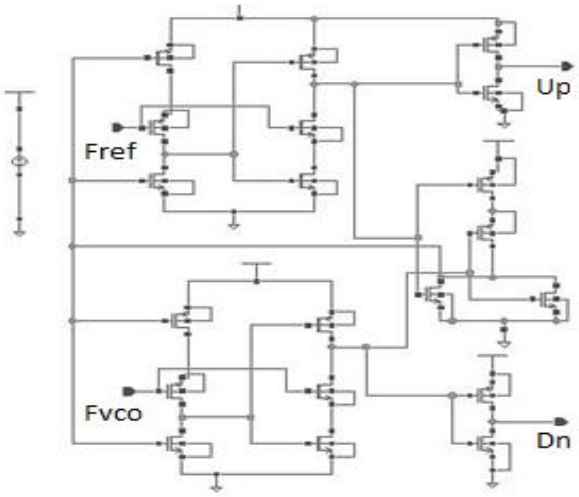

Fig. 8 Schematic diagram of Phase Frequency Detector

Phase frequency detector is a circuit which has two inputs, which can detect both the frequency and phase differences and its output, is feedback to the charge pump. When the reference frequency (F_{ref}) and VCO frequency (F_{vco}) inputs are unequal in frequency and/or phase, the differential UP (Up) and DOWN (Dn) outputs will provide pulse streams. Its subtraction and integration provide an error voltage for control of a VCO

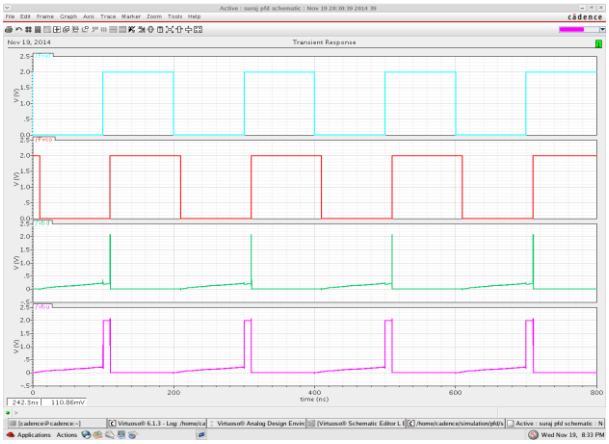

Fig. 9 Transient response of phase frequency detector

Here after simulation we find that by providing two inputs that is, if initially Dn = Up =0 then a rising transition on F_{ref} leads to Dn = 1, Up =0. The circuit remains in this state until F_{vco} goes high, at which point Dn return to zero. The behavior is similar for the F_{vco} input. The two inputs have equal frequencies but F_{ref} leads F_{vco}. The output Dn continues to produce pulses whose width is proportional to difference in phase of Up and Dn. The output of the PFD depends on both the frequency and phase of the inputs. This type of the phase detector is also termed as the sequential detector. Phase Frequency detector (PFD) is a digital circuit detecting phase or frequency difference between reference clock and voltage controlled oscillator (VCO) clock/feedback signal and generates output signal if frequency of VCO is to be decreased or increased. The PFD circuit should consume low power and have a minimum dead zone. Dead zone is a region wherein a PFD fails to detect small frequency/phase errors.

Charge pump is the next block to the phase frequency detector. The output signal is generated by the PFD is directly inserted to the charge pump. The main purpose of a charge pump is to convert the logic states of the phase frequency detector into analog signals suitable to control the voltage-controlled oscillator (VCO). Basically, the charge pump consists with current sources and up & down signals. The output of the charge pump is connected to the VCO that integrates the charge pump output current to an equivalent VCO control voltage (V_{ctrl}) [8]. Charge pump circuit is an important block of the whole PLL system. It converts the phase or frequency difference information into a voltage, used to tune the VCO. Let us assume that T_{in} be the input period and a charge pump provides a current of $\pm I_p$ at t=0, the phase of F_{vco} by Φ_0, i.e, $\Delta\Phi = \Phi_0$ u(t). as a result F_{ref} and F_{vco} continues to produce pulses that are $\Phi_0 T_{in}/(2\Pi)$ second, thus V_{out} can be expressed as

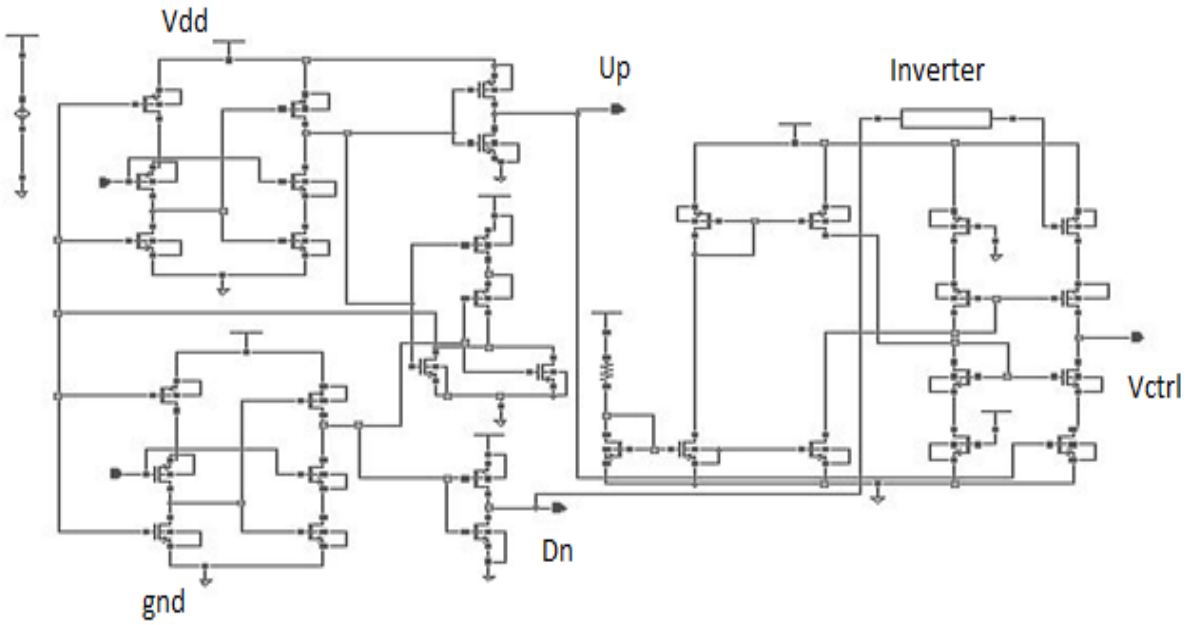

Fig.10 PFD with Charge Pump Circuit

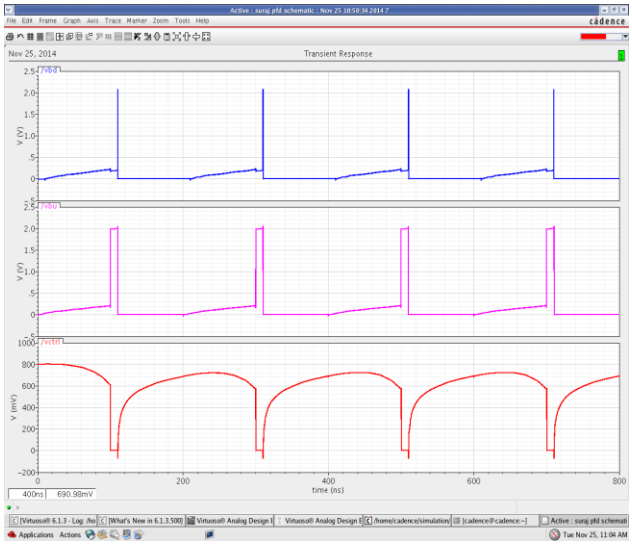

Fig.11 Transient response of PFD with Charge Pump

$$V_{out}(t) = \frac{I_p}{2\Pi C_p} t.\Phi_0 u(t) \qquad (1)$$

The impulse response of Equation (1) is expressed as

$$h(t) = \frac{I_p}{2\Pi C_p} u(t), \qquad (2)$$

yielding the transfer function of Equation (2)

$$\frac{Vout}{\Delta\Phi}(s) = \frac{I_p}{2\Pi C_p} . \frac{1}{s} \qquad (3)$$

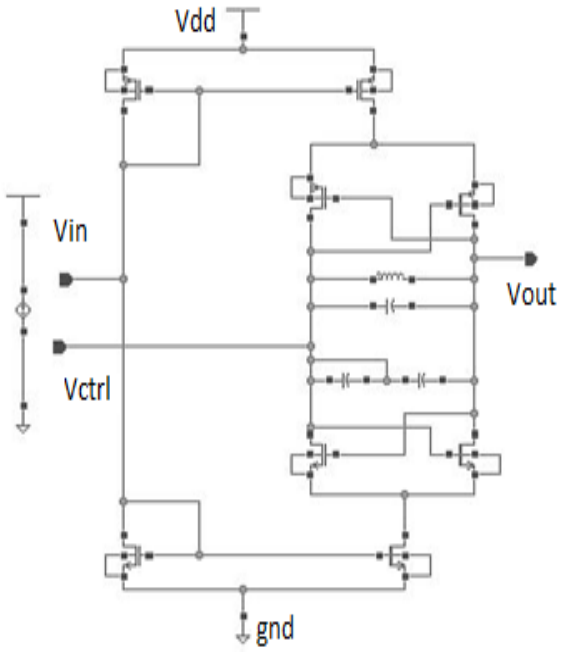

Fig. 12 Schematic diagram of VCO

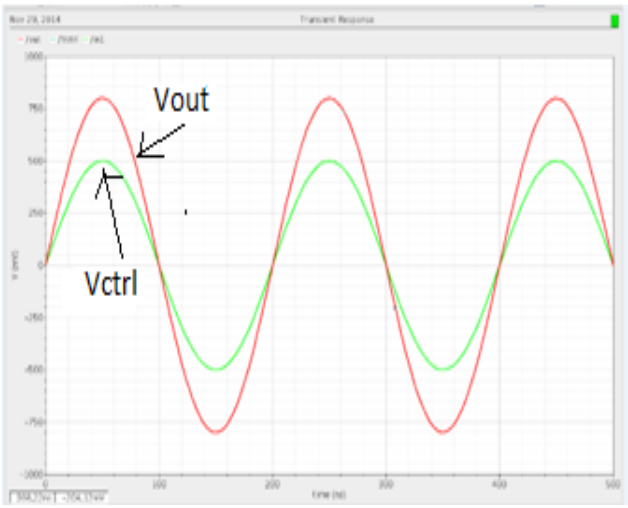

Fig.13 Transient response of VCO

Voltage controlled oscillator is the basic building block of PLL. By controlling the input voltage (V_{ctrl}) we can control the output voltage of VCO, here in this circuit output of charge pump is feedback to the input of the VCO to generate the output voltage which has, low noise, wide tuning range and higher linearity. The transconductance of VCO is represented as

$$g_m = u\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{th}) \qquad (4)$$

Where, μ_n is the permittivity C_{ox} is the oxide Capacitance W is channel width and L is channel length. The parameter V_{gs}, V_{th} are the input and threshold voltage.

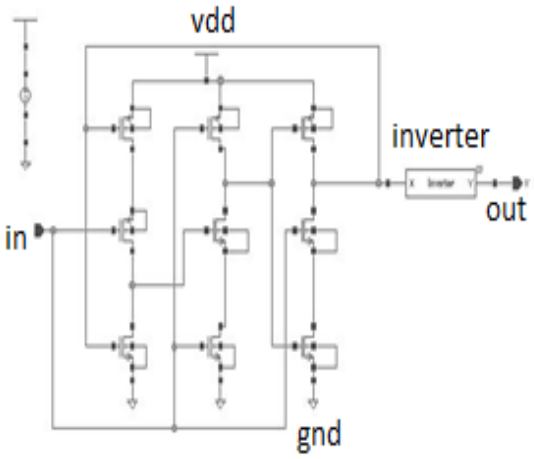

Fig.14 Schematic diagram of divide-by-2 frequency divider

Frequency divider circuit is used to provide the feedback path in the PLL. It takes the output of VCO as an input frequency F_{in} and produced an output signal of a frequency F_{out}.

$$F_{out} = \frac{F_{in}}{n} \quad (5)$$

Where n is the integer. It is used to multiply the frequency of F_{ref} for frequency synthesizer. Fig 14 shows that the divide-by-2 frequency divider and must operate at higher frequencies and obtain a 50% duty cycle at output frequency [2]. As the VCO is operated in the multi-GHz range, the PLL requires high frequency dividers, which converts high frequency to the low frequency and can be compared to the reference frequency.

3. COMPARISION TABLE

SPEC	**This study**	**Shao and Fu-Jen (2013) [2]**	**Park and Park (2009) [4]**	**Liu and Shi (2008) [5]**	**Chiu et al. (2007) [6]**
Technology	45nm	0.35um	0.18um	0.35um	0.18um
Supply Voltage	1.0	3.3	1.8	3.3/5	1.8
Output frequency	5.0 GHz	1.68 GHz	1.49 GHz	2.0 GHz	5.47-5.65 GHz
Loop bandwidth	NA	30KHz	NA	NA	40KHz

4. SIMULATION RESULTS & DISCUSSION

In this paper, the concept of phase locking and details of phase locked loops and its building blocks are explained. Simulation results of PFD are shown in Fig.4, Fig.5, Fig.6, and Fig.7 at different phases at 0^0, 90^0, 180^0, and 270^0 respectively. Fig. 9 shows the transient response of phase frequency detector. Fig.11 shows the transient response of PFD with Charge Pump. Fig.13 demonstrates the transient response of VCO at 5.0 GHz frequency.

5. CONCLUSION

The proposed CMOS PLL is simulated in CADENCE virtuoso 45nm CMOS technology**.** The output clock generated for a frequency of 5.0 GHz. The time taken for the PLL to lock to the reference frequency is 500ns. The voltage supply is applied to the circuit is 1 volt and is stable in the acquisition period. Phase locked loops are widely used in the application of frequency multiplication and synthesizers of RF transceivers, skew reduction, jitter reduction etc.

6. ACKNOWLEDGEMENT

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