Body Biasing Scheme to Control Leakage, Speed and Stability in SRAM Cell Design

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ABSTRACT
In this paper a new SRAM cell is designed with a body bias controller to control leakage, speed and stability. A novel controller circuit is proposed to control the value of threshold voltage. Operation of the proposed controller is based on word line signal levels. In order to reduce sub threshold leakage current, the NMOS access and driver transistor is adjusted to a higher threshold voltage. Similarly, threshold voltage of NMOS access transistor is adjusted to a low value for improved read and writes speed. As compared to conventional 6T SRAM cell, the proposed design reduces the leakage power by about 52.27%, when tested on (8×16) SRAM cells.

Keywords
Leakage power dissipation, sub threshold current, power gating, sleep transistor and transistor stacking

1. INTRODUCTION
In today's system on chip (SoC) era, memory becomes an important design component due to increasing use of memory content in SoC chips. About 90% of the area is occupied by memories with different functionality.

In today's electronic system [1], SRAM's play a vital role of temporary storage in modern microprocessor, microcontrollers and computers etc.

System on chip (SOC) requires both low power consumption and high operating speed because SRAM covers a significant portion of the total die area as reported in international roadmap semiconductor (ITRS) [2]. Power dissipation becomes one of the important factors that affect the circuit performance as device scales down to deep sub-micron regime. Researchers have already proposed that the sub threshold SRAM cell would be the possible design option to reduce power consumption [3].

Continued device scaling led to excessive leakage and now it is comparable to active power dissipation.

Leakage power consumption is the dominant contributor in SRAM cells.

Lowering of supply voltage is achieved by technology scaling but this has many challenging obstacles such as reduction in read static noise margin (RSNM), write static noise margin (WSNM) and operating speed [4-5]. Stability in SRAM cell is caused by the mismatch in threshold voltage of cross-coupled inverter pair [6]. Reduction in supply voltage also reduces SRAM cell current, which consequently decreases the speed of cell.

To solve the problem of static noise margin a FD-SOI device is proposed in [7], but its high cost and difficulty in manufacturing limits its usage. So variation of Vth is the main problem and to solve this problem bulk MOSFET is highly desired. Bulk voltage in CMOS technology cannot be changed abruptly because if reverse bias voltage of PN junction increases after certain limit, then it will increase the leakage current, band-band tunneling and consequently damage the transistor. So it is important to optimally control the threshold voltage of the transistor for minimum leakage, high speed and good stability. SRAM cell consist of four NMOS transistor (two-access transistor & two-driver transistor) and two PMOS-load transistors as shown in Fig.1. As indicated in the figure, maximum amount of leakage is passed through the NMOS transistor that is from Vdd to ground (dashed line in red) and bit-line to ground (dotted line in red) [8].

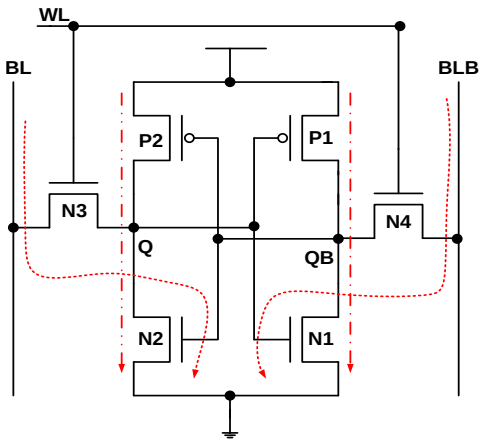

Fig. 1. Leakage path in 6T -SRAM cell

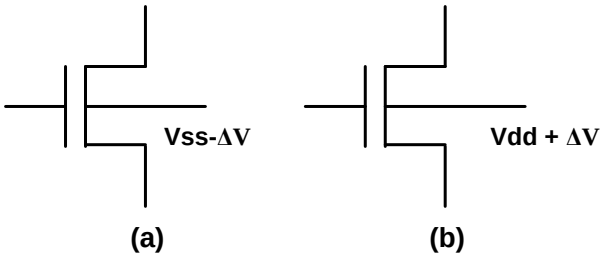

Fig. 2. Body bias voltage of NMOS transistor in (a) standby mode (b) active mode

The speed of the cell can be enhanced by forward body-biasing the NMOS access transistor (N3&N4) in active mode. In reverse body-bias, threshold voltage of a transistor becomes high and with foreword body bias threshold voltage of a transistor becomes low. These two performances metric can be achieved by over-driven body-bias which causes the body voltage to move further beyond the supply rail as shown in Fig. 2 [9].

A typical memory organization consists of individual cells arranged in an array of horizontal rows and vertical columns [10]. Based on word line signal, a particular row of the cell is in active mode and others are in standby mode.

In this paper, we propose a word-line based controller circuit to operate the SRAM cell in active and idle mode. The word line signal defines the two different body voltage for NMOS and PMOS transistor in active and idle mode.

The remainder of the paper is organized as follows. Section II discusses the related work. Section III discusses the proposed SRAM cell. Section IV analyzes the results of proposed cell. Finally section V concludes this paper.

2. RELATED WORKS

In [11] a cell called PP-SRAM (Fig.3) is suggested in order to reduce gate leakages. PMOS access transistors have been used instead of NMOS access transistor. The mobility of holes is less than electrons, so PMOS transistor would cause a reduction in timing performance. To compensate this reduction width of PMOS transistor is wider than NMOS transistor is chosen. Further, in this design a higher threshold voltage for PMOS transistors is used to reduce the sub threshold leakage current, while, in order to compensate for performance reduction caused by application of high threshold voltage transistor, a forward body biasing method is used. The body bias voltages of all the four load and access transistors P1, P2, P3 and P4 are set to Vdd/2 in order to enhance the timing performance in active mode. This in turn causes forward body bias and hence results in reduction of threshold voltage, improvement of performance but may lead to increased leakage power consumption.

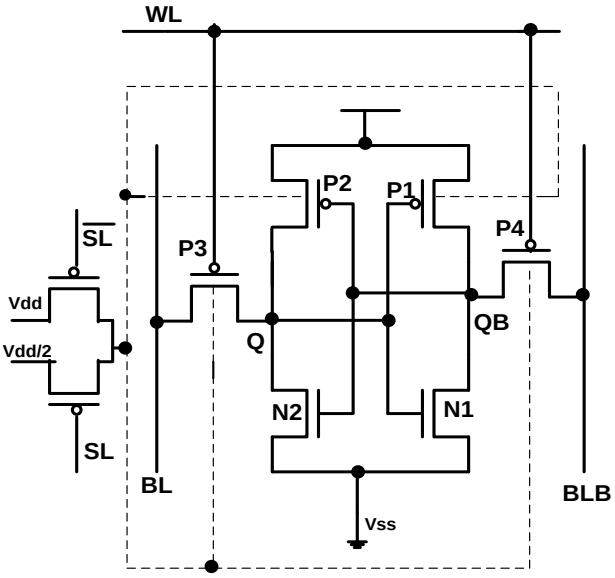

Fig. 3. PP-SRAM cell

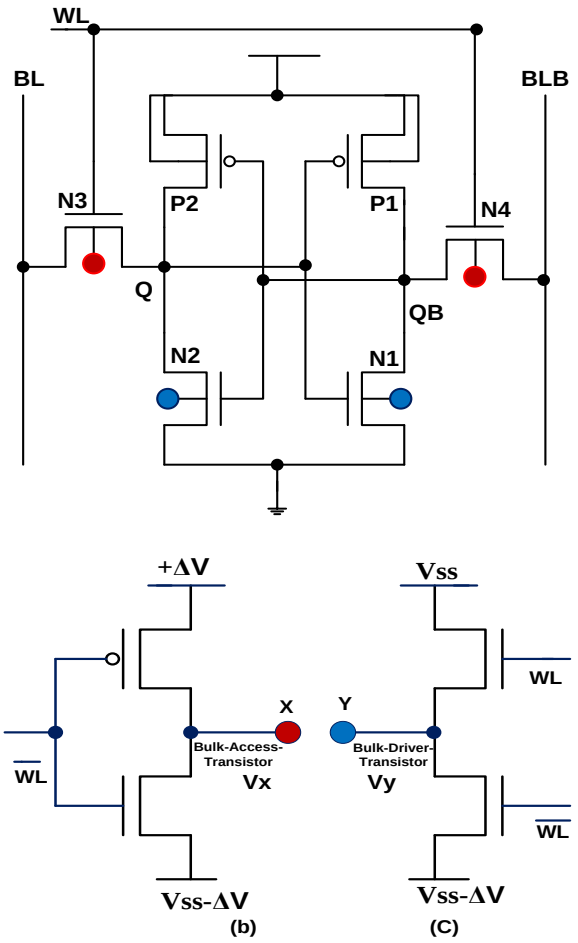

Fig. 4. Proposed body bias Controller with SRAM cell

3. PROPOSED CONTROLLER DESIGN

This section presents the 6T-SRAM cell with the proposed controller circuit. The controller circuit as shown in Fig.4 is designed with minimum number of transistors which help in improving the speed during active mode and reduce leakage power during standby mode. In the array of SRAM cells, the body bias voltage of NMOS access and driver transistor is controlled by word line signal. To control the leakage, speed and stability, different voltages levels are applied at the body during active and standby mode.

In the Fig. 4, red node indicates body bias voltage for NMOS-access transistor and blue node indicates body bias voltage for NMOS-driver transistor. In standby mode, word line signal WL = 0 and WL (bar) = 1. The X-node (red node) of body bias controller in Fig. 4(b) transfers Vss-ΔV to the body of NMOS-access transistor. Similarly Y node (blue node) in Fig. 4(c) transfers Vss-ΔV to the body of driver transistor. These body bias voltages provide a high threshold voltage to both NMOS driver and access transistors, which consequently reduces the leakage current.

During active mode, WL = 1 and WL (Bar) = 0 , which enables X-node to transfers small body-voltage (+ΔV) to NMOS access transistor and enables Y-node to transfer Vss = Gnd voltage to the body of NMOS driver transistor. The NMOS-access transistor is now forward body biased and causes a low threshold voltage, which consequently enhances the read/write speed. On the other hand, driver transistor will

get no-body bias (because of ground potential to the bulk of NMOS transistor). To avoid the stability problem we are keeping no body bias to load and driver transistors in active mode because VTH variation of driver transistor has the largest impact on the voltage transfer characteristic shape. Thus W/L ratio of driver transistor is large compared to other transistors in SRAM cell as in [12]. The combination of SRAM cell and controller circuit provides good operation during active and standby mode. To test the functionality of the circuit we have chosen $+\Delta V = 0.4V$ and $Vss - \Delta V = -0.23V$, Vss = ground and Vdd = 1V at 65nm technology. Depending upon the word line signal value WL=1(0), the control circuit transfers voltages to the body of NMOS access transistor as Vx = 0.4v or $Vss-\Delta V = -0.23V$ respectively. Similarly, for NMOS driver transistor, the control circuit transfers a voltage to the body as Vss = ground (0V) and $Vss-\Delta V = -0.23V$ respectively when WL = 1(0). Based on these values the simulated waveform of the control circuit is shown in Fig.5. Array structure with the proposed controller is shown in Fig.6. The control lines from controller circuit are indicated in blue and red colors, which are shared by the row of cells.

4. RESULTS

To verify the proposed design, extensive simulations with Tanner EDA tool using a 65nm predictive technology model (PTM) [13] are performed. The performance matrices of the proposed SRAM cell are compared with conventional SRAM cell using 1V supply voltage.

A. Static power dissipation

Static power dissipation of the circuit is measured during standby mode. In standby mode, bit line pairs are charged and word line signal is zero which turns -off the access transistors. The driver and access transistors are overdriven by applying Vss–ΔV to the body of NMOS transistor. Table 1 shows the static power dissipation at different threshold voltages.

Table 1. Static power dissipation

8× 16 Array = 128 cells (27^0C)		
SRAM cells	**Static power (W)**	**% saving**
Conventional 6T	0.0023911	------
Proposed design	------	------
Vx & Vy	------	------
-0.1v	0.0016846	29.54%
-0.16v	0.0015998	33.09%
-0.23v	0.0015055	37.03%
-0.28v	0.0014412	39.71%
-0.32v	0.0013915	41.80%
-0.36v	0.0013433	43.82%
-0.41v	0.0012859	46.25%
-0.45v	0.0001165	51.27%

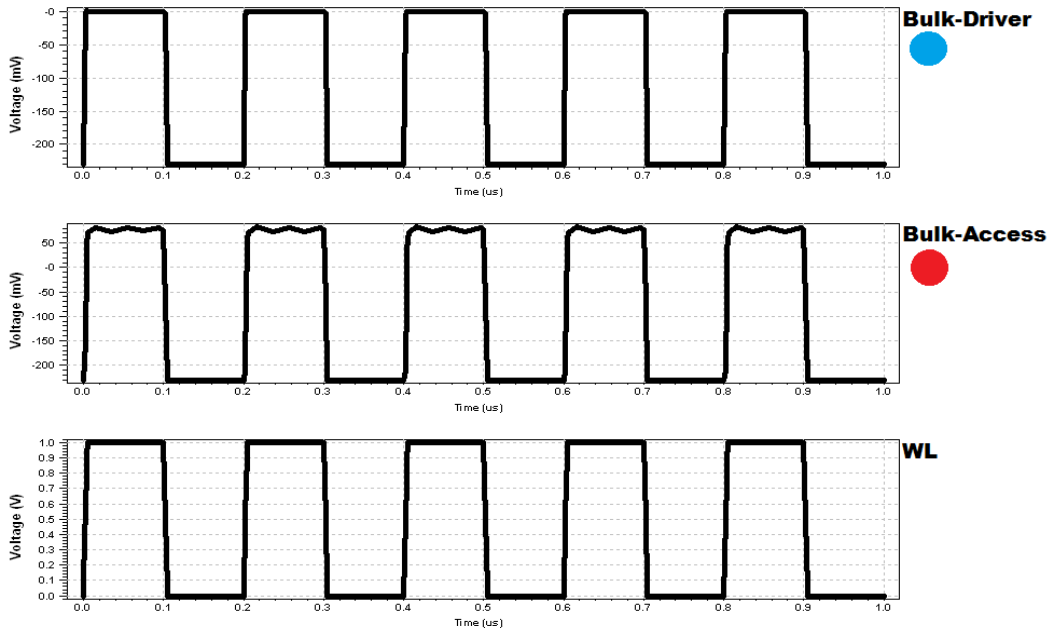

Fig. 5. Control signals to the body of access and driver transistor

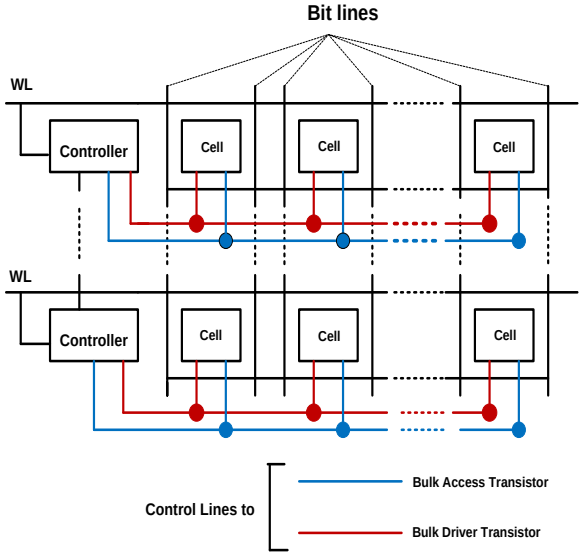

Fig. 6. Array structure of proposed design

In this way threshold voltage of each of NMOS transistors (N1, N2, N3, N4) is raised to a high value, which will reduce leakage current in SRAM cell. Simulation is carried out at different temperature of 250C , 500C , 750C and 1000C. Power consumption in the proposed circuit is then compared with the conventional SRAM cell and are shown in Table 2. Fig.7 & 8 shows the static power dissipation at different temperature and process corners.

Table 2. Static power dissipation at different temperature

Temp	Conventional	PPSRAM	-0.23v
25	1.0428E-005	1.0214E-005	8.7125E-006
50	1.1555E-005	1.0535E-005	9.5878E-006
75	1.2898E-005	1.02873E-005	1.0627E-005
100	1.4509E-005	1.04478E-005	1.1869E-005

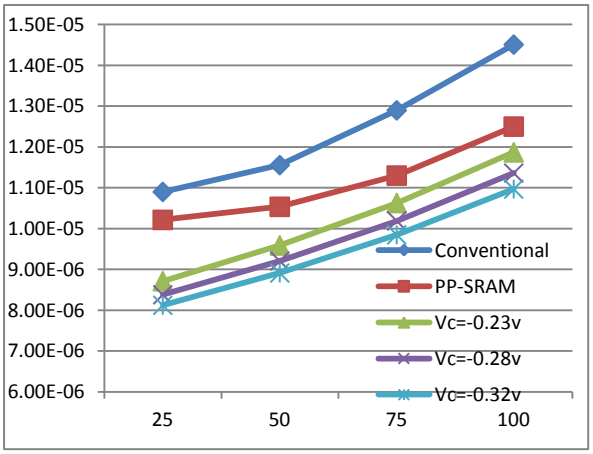

Fig. 7. Static power at different temperature

B .Read and write delay

Read and write delay of SRAM cell is measured when word line is activated. In the architecture of proposed cell as shown in Fig.4 and Fig.5, the control circuit transfers a small voltage Vx = +ΔV through X node (red node) to the body of NMOS-access transistor. This forward body bias will reduce the threshold voltage of NMOS transistor which enhances the read and write speed.

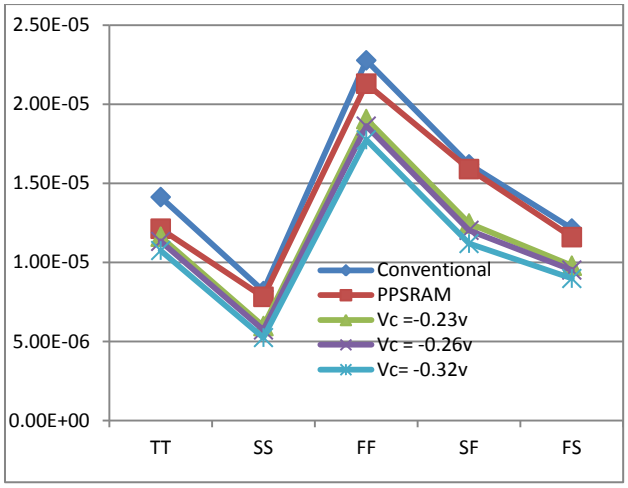

Fig 8. Static power at different process corners

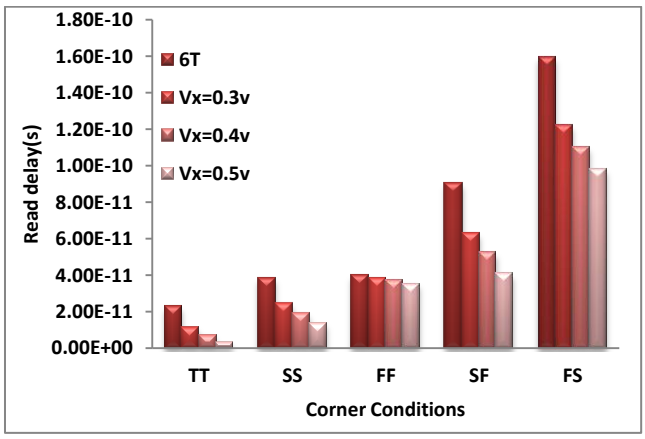

Fig.9 Read delay at different process corners

On the other hand, Y node (blue node) transfers Vy = Vss (ground) to the body of NMOS driver transistor which keep the transistor in no-body bias (i.e. body is tied to ground) state.

Read and write delay of the circuit is calculated over a wide range of forward body-bias, Vx = 0.3V to 0.5V. It is seen that the proposed design gives a better read and writes performances over conventional 6T SRAM cell at different process corner as shown in Fig.9 and Fig.10. Simulation shows better read and write performance obtained at Vx = 0.5V.

C .Static noise margin

Beta ratio of conventional 6T and proposed SRAM cell is taken as 1.8. The W/L ratio of driver transistor is large as compared to all other transistors in SRAM cell. Fig.11 shows the simulated butterfly curve during read operation.

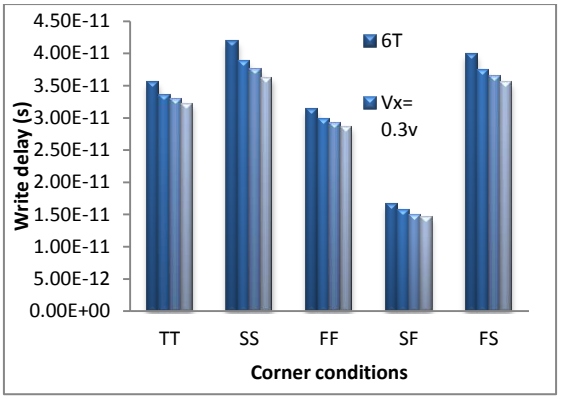

Fig.10 Write delay at different process corners

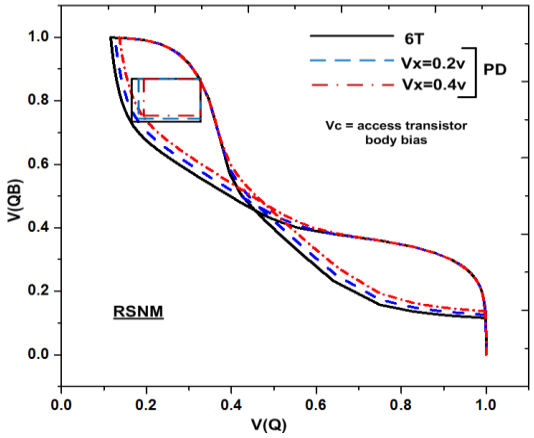

Fig.11 Static noise margin during read operation

During active mode, Vx node supplies positive voltage to the body of NMOS access transistor. So VTH voltage of NMOS transistor decreases. This decrease in VTH voltage has negative impact on read SNM. As Vx voltage gradually increases stability decreases a little and the size of the lobes get smaller. The threshold voltage of driver transistor in the proposed SRAM circuit is unaltered, which means it is set to Vss = ground. This is because a change in threshold voltage of driver transistor during active mode changes the shape of voltage transfer characteristic. The read static noise margin of 6T SRAM cell obtained is 162.32mV and read SNM of proposed design is degraded by 156.26mV at Vx = 0.2V.

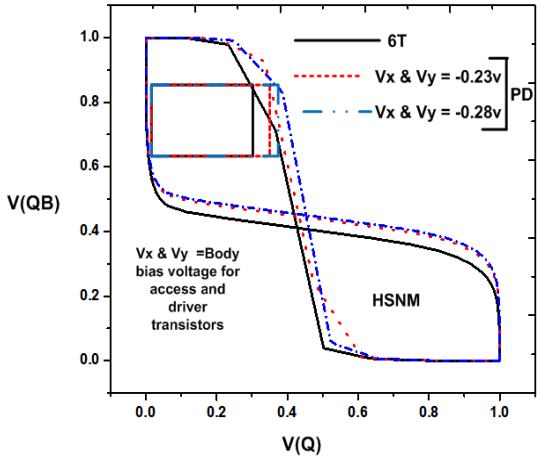

Fig.12 Static noise margin during standby operation

Comparison of static noise margin of conventional and proposed design is shown in Fig.12. In standby mode, threshold voltage of all the transistors are high , so the transistor is less leaky and hold noise margin (HSNM) improved. We can see from the curve as the body bias voltage increases towards negative value, the curve getting expanded, which means better hold static noise margin. For instance, with Vx and Vy = -0.23V , hold SNM of the proposed cell is 424.9mV , whereas it is 356.9mV in conventional 6T SRAM cell.

5. CONCLUSION

In this paper a new controller circuit is proposed which works on the word line signal level. The control circuit reduces leakage, delay and maintains the stability in SRAM cell by controlling the threshold voltages. In standby mode static power consumption is reduced by 51.2% in 8×16 array. Furthermore, the hold SNM performance is enhanced by controlling the threshold voltage. Whereas, the reduction in read static noise margin is also within the acceptable range.

6. REFERENCES

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