Designing Equivalent Model of Floating Gate Transistor for Smart Dust in Rural Areas

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ABSTRACT
In this paper an equivalent model for floating gate transistor has been proposed for smart dust. Smart dust has an advantage of discrete size with substantial functionality and connectivity so; it will provide new methods to sense and interact with the environment especially in rural areas .Using the floating gate voltage value, capacitive coupling coefficients has been found at different bias conditions. The proposed model can be extended to the transient conditions as well. The SPICE equivalent model is designed and current voltage characteristics and Transfer characteristics are comparatively analyzed.

Keywords
FGMOS, floating gate transistor, capacitive coupling coefficient, smart dust

1. INTRODUCTION
Electron tunneling mechanism was proposed to be used for programming and erasing the proposed cell using a thin insulator layer (having thickness less than 5 nm). But fabrication of thin oxides was not possible then [1]. The first floating gate device with a thick gate oxide was introduced by Frohman Bentchowsky [2]. It was called FAMOS (Floating Gate Avalanche Injection Metal Oxide Semiconductor). Then FLOTOX (Floating Gate Thin Oxide) Memory cell [3] and ETOX [4] structures were proposed. FLOTOX cell contained a thin oxide layer so that the programming and erasing was done by Fowler Nordheim tunneling. The combination of Hot Electron programming and Fowler Nordheim tunneling was used in ETOX (EPROM Tunnel Oxide) cell. It had a thin oxide layer.

2. PROPOSED MODEL OF FLOATING GATE FOR SMART DUST
A smart dust element is a self-contained sensing and communication system that can be combined into roughly a cubic-millimeter mote to perform integrated, over sensor networks [4]. Smart dust can consist of hundreds to thousands of dust motes, each containing the capability of sensing and monitoring and communicating to other devices. Each mote contains more than individual sensor, a power supply, circuitry, bi-directional communication, and a microprocessor. Advances in miniaturization, integration, and energy management in digital circuit, optical communications and Micro Electro-Mechanical Systems (MEMS) led to the manufacturing of small sensors, optical communication components, and power supplies, whereas microelectronics provides increasing functionality in smaller areas, with lower energy consumption [4,5].Dust motes can be mounted to large collection of motes can just be deployed over the environment at random. The motes obtain the desired information from the surrounding environment .Depending on the application, dust motes can be made to only communicate directly with a base station transceiver, or peer-to-peer communication can be performed between dust motes. Smart dust has applications for industry as well as the military. Useful applications for smart dust includes; Collecting data for meteorological, geophysical, or planetary research , Tracking the movements of birds, small animals, and even insects , Monitoring product quality - temperature, humidity, pressure sensors and Defense-related sensor networks - acoustic, vibration, and magnetic field sensors[6]. The design of a bidirectional free-space optical communication link in which a base station transceiver communicates simultaneously with a collection of many dust motes includes Image sensor [6]. In this paper, floating gate transistor has been proposed for smart dust. The block diagram of proposed work has been shown in figure 1[6].

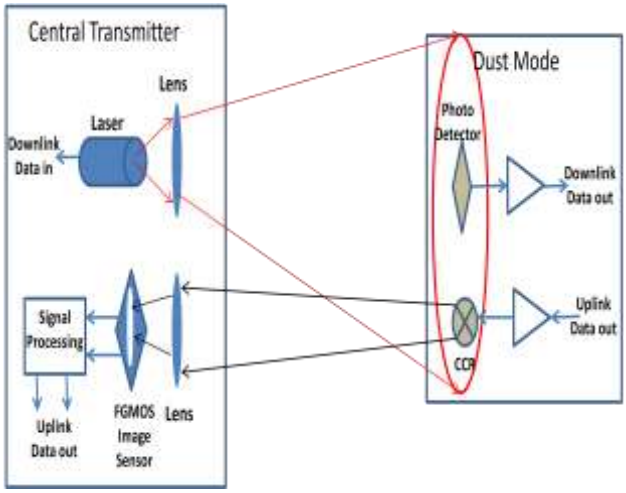

Figure 1: Block diagram of proposed work [6]

In figure 1, CCR represents micro fabricated corner cube Retroreflector, it reflects any incident ray of light within a certain range of angles. A special MEMS structure on the uplink side, makes it possible for dust motes to use passive optical transmission techniques by using the corner-cube retroreflector (CCR) approach. A high frame-rate FGMOS imaging system at the base-station transceiver captures these CCR signals as light blinking on and off. It decodes these blinking images to yield the uplink data. The base station receiver contains an imaging receiver with a lens and FGMOS image sensor array. The imaging receiver uses periodic pulsation of the downlink for synchronizing the transmission from all dust motes to the frame clock of the imaging array. In this proposed model FGMOS has been demonstrated for smart dust motes.The most common approach for modeling a floating gate transistor is the capacitive coupling approach. Using the capacitive coupling approach, the Floating Gate potential comes out to be a function of not only the control gate voltage, but also the source, drain and bulk potentials.

$$V_{FG}= \alpha_G V_{GS}+ \alpha_D V_{DS}+ \alpha_S V_S+ \alpha_B V_B \qquad (1)$$

The Floating gate potential is given by the equation (1)

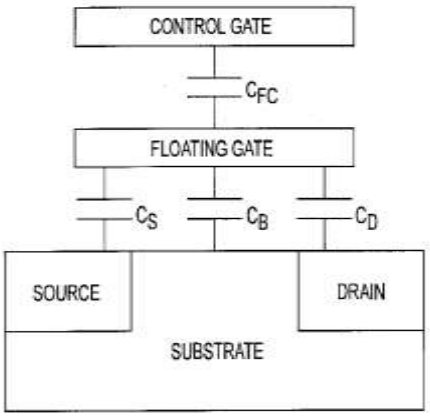

Figure 2: Schematic cross section of a Floating Gate Transistor [7]

Figure 2 shows the schematic cross section of a floating gate transistor. Different methods have been devised in literature for determination of coupling coefficients [8-15]. These methods can be classified into three categories:

i. Dummy cell approach
ii. The Floating gate cell approach
iii. A new method without using coupling coefficient approach

3. IMPLEMENTATION OF SPICE EQUIVALENT MODEL

Implementation of the SPICE equivalent model has been done using Tanner tools. The SPICE equivalent model proposed here is a hybrid of the two schemes: The capacitive coupling approach and the method proposed in [15] using the charge balance equation. The capacitive coupling approach has been shown in figure 3.

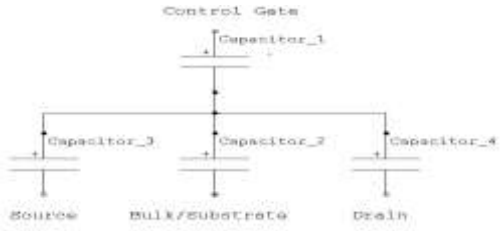

Figure3: Capacitive coupling approach

It uses a capacitive circuit to represent the equivalent circuit for an FGMOS. Another method based on finding the zero of charge balance equation at the Floating Gate node [12] has been shown in figure 4.

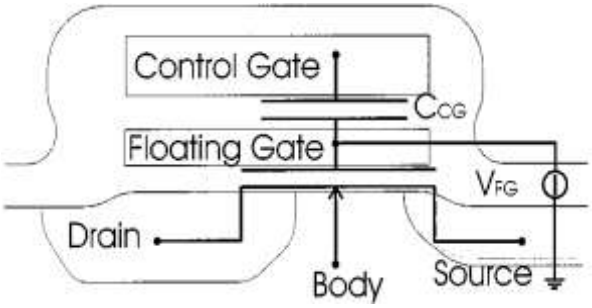

Figure 4: Compact model for an FGT proposed in [15]

A MOSFET is present and a capacitor is also present. Since the floating gate node has been initialized to a potential value explicitly, there is no problem of solving the capacitive net, which SPICE like simulators are unable to do. The problem with this model is that in many simulators, such provisions as embedding the code in a voltage source do not exist. This model is slow because the algorithm is repeated for all combinations of bias conditions. Moreover, the charge on the floating gate has to be calculated using the base MOSFET model used. So, a thorough knowledge of all the parameters of the model is required. The charge calculation procedure cannot be implemented in a simulator. For modeling of floating gate devices, the accurate knowledge of floating gate voltage is necessary which can be efficiently calculated by this method for required bias conditions. Having determined the floating gate voltage, the coupling coefficients can be calculated using the equation (2).

$$V_{FG} = \alpha_G V_{CG} + \alpha_D V_D + \alpha_S V_S + Q/C_T \quad (2)$$

Calculating the coupling coefficients since floating gate potential value can be found for a particular technology at the bias conditions during read, program and erase. By using those values, the values of the capacitors can be found out (the value of interpoly capacitor is known). To handle the problem of capacitive net, resistances have been incorporated in parallel. The proposed model is as shown in Figure 5.

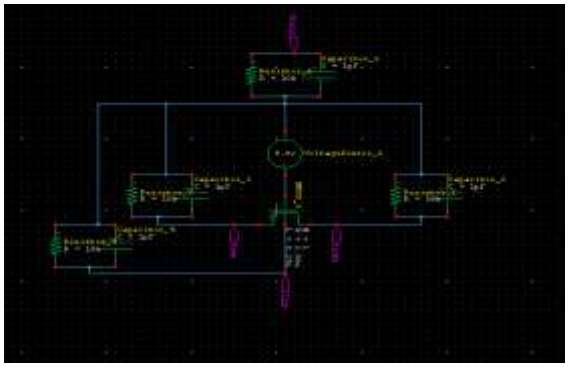

Figure 5: SPICE equivalent model

Where, VoltageSource_1 is V_{CG}, VoltageSource_2 is V_{DS} The Floating gate potential is referred as V_{FG} in equation (1). This model also contains an input node that can be defined as a dc voltage source in T-SPICE. In case any charge is present on the Floating gate, it is modeled using this dc voltage source. This model can be used for analog and digital circuits.

4. RESULTS AND ANALYSIS

The dc current voltage characteristics as well as dc transfer characteristics have been plotted for an FGMOS with W/L=0.25µm/0.375µm, inter poly capacitance of 0.8fF for both programmed and erased states. The results obtained are accurate as compared to the capacitive coefficient coupling methods described earlier.

4.1 Current Voltage Characteristics

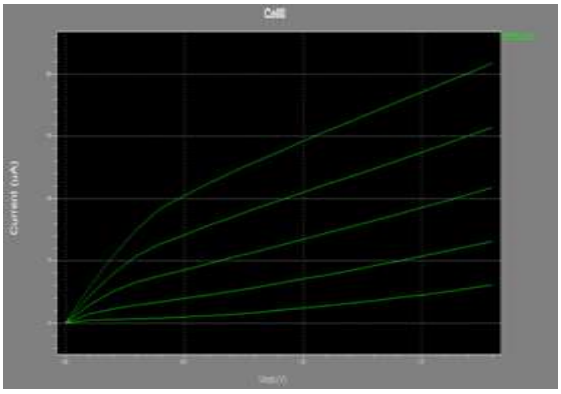

Figure 6: I-V characteristics for FGMOS in the programmed state

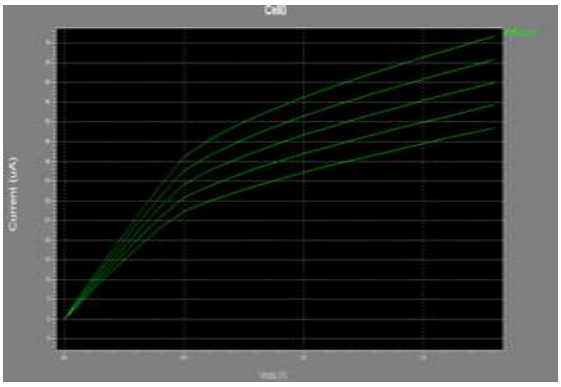

Figure 7: I-V characteristics for FGMOS in the erased state

In this particular state, it has been assumed that the charge stored in the floating gate is zero. However, this is not the case. A small amount of residual charge is always present on the floating gate that needs to be modeled. The magnitude of current with same applied bias is more for the erased state as can be interpreted from the graphs. The transfer characteristics also have been obtained for an FGMOS for both programmed and erased states with W/L=0.25µm/0.375µm, inter poly capacitance of 0.8fF.

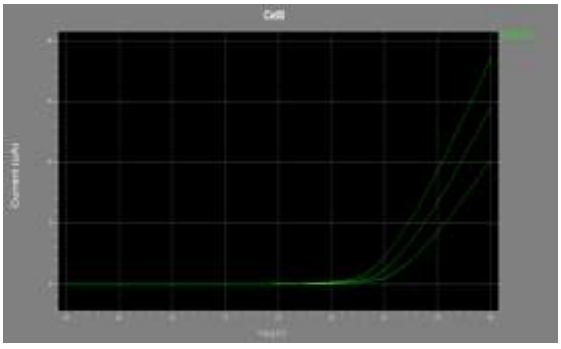

Figure 8: Transfer characteristics for FGMOS in the programmed state

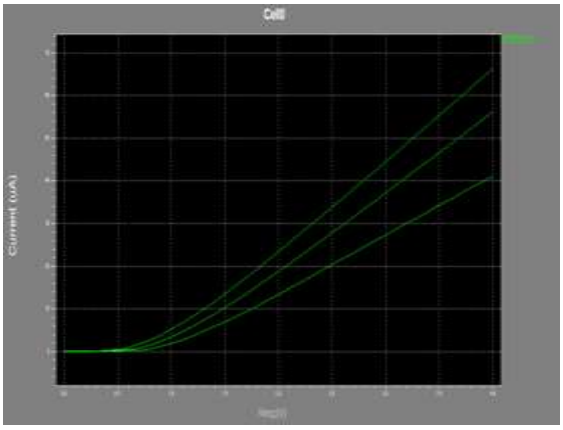

Figure 9: Transfer characteristics for FGMOS in the erased state

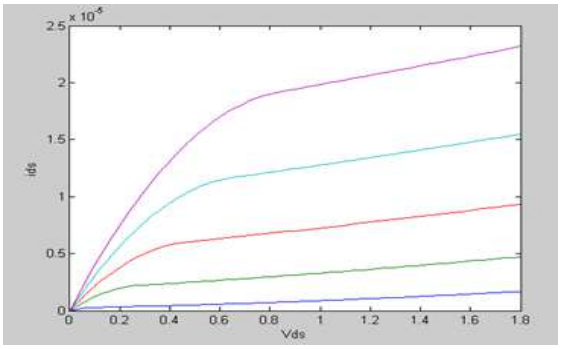

Figure 10: I-V curves of FGMOS with W/L=0.25µm/0.375µm, inter poly capacitance of 0.8fF

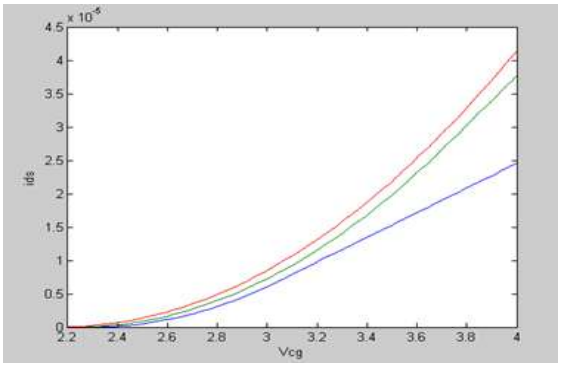

Figure11: Transfer curves of FGMOS with W/L=0.25µm/0.375µm, inter poly capacitance of 0.8fF

The graphs shown in figure 6 and figure7 are represented the programmed state, the graphs shown in figure 8 and figure9 are of Erased state and graphs shown in figure 10and figure 11 are represented the transfer characteristics.

5. CONCLUSIONS

The proposed model is faster and requires much less expertise than the one proposed in [15]. It is accurate than the original capacitive coupling approach since the capacitive coupling coefficients are extracted using the algorithm based on the charge balance equation proposed in [15]. Being a hybrid of the two schemes, it is better than both. This proposed model is designed for improving the number of dust motes. This model when used in base station receiver side will enhance the performance of the smart dust.

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