A Cost Effective Built-in-Self Test for Second Order Sigma Delta Modulator

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ABSTRACT
Testing of high resolution second order sigma delta (ΣΔ) modulator is a very expensive process. With the advanced technology, where the complexity over a small area is increasing, then testing at low cost with good accuracy is becoming a tedious issue for the manufacturing process. The cost effectiveness can be calculated on the basis of different parameters of the ΣΔ modulator such as SNDR, ENOB, Gain, Offset, THD, SNR etc. Testing time also play an important role in the cost effectiveness of the modulator. The Built-in-self-test (BIST) allows the machine or circuit to test itself. BIST is desirable for the VLSI system in order to reduce the cost per chip of production –time testing by the manufacture, it can also provide the means to perform in-the field diagnostic. Therefore, this paper will demonstrate a possibility to simplify modeling and simulation of testing strategy of high-resolution ΣΔ modulator using MATLAB SIMULINK environment. Here, we are finding the cost effectiveness on the basis of Signal to Noise Distortion Ratio (SNDR) for the ΣΔ modulator BIST. A ΣΔ modulation based signal generator is considered which can produce analog sinusoidal test stimuli and digital reference signal on chip. By comparing the ADC output with that of the generator reference signal, the parameter can be determined on chip based on the standard equations in the proposed simulation environment.

1. INTRODUCTION

1.1 Over Sampling definition
Sampling at a higher rate which is a larger multiple of normal Nyquist rate. The sigma delta conversion techniques are currently more widespread used due to the latest advancement in the technology. The converters are basically used in the applications like in the communication systems, in industries for the weight scales and for precise measurement. Analog to digital converters are driven by the increasing demand of signal bandwidth and dynamic range in these applications. These architectures span a range of intended resolutions and conversion speeds.

1.2 Application Areas of Sigma Delta ADC
It can be used for wireless and wire line communication and its most efficient use is in the audio applications in which frequency range is from 20 Hz to 20 KHz and it gives better resolution.

1.3 Other Application Areas
Oversampling ADCs are traditionally used in instrumentation, seismic, and audio applications, with low signal bandwidth and high resolution. In recent years, due to improvements I CMOS technology and architecture or circuit design techniques, ADCs can achieve higher input signal bandwidth and medium to high resolution (12–16 bits), and have a wide deployment in wireless and wire- line communication applications, one of the challenges in these techniques is how to achieve high resolution, high performance and less consuming power with smaller hardware cost.

Over the last year high-resolution analog-to-digital conversion based on ΣΔ modulation due to advantages of digital processing (e.g. noise immunity, design automation), has become common place in many measurement applications including seismic, biomedical and harsh environment sensing & also having high demand in the market for precision audio, high-definition video and targeting micro-power medical devices such as hearing aids devices, silicon condenser microphones play an increasing role in applications as mobile phones, laptops, and wireless communication industry it is necessary to have ADCs operating with very low power dissipation. Oversampled Sigma Delta modulation has gained much popularity in the analog to digital conversion application for their good performance in low frequency, low consumption, low supply voltage and low silicon area occupation. One of the challenges in these techniques is how to achieve high resolution, high performance as well as less consuming power with smaller hardware cost. For achieving these challenges second order continuous time band-pass sigma delta ADC have been used. ADC based on second order sigma-delta modulators is attractive for VLSI implementation because they are tolerant of circuit non-idealities and component mismatch. However, issues such as clock jitter and excess loop delay become great challenges for the designer, especially at high sampling frequency.

With the modulator's robustness to the imperfection of analog implementation, the sigma–delta modulator is suitable for integrated circuits implementation especially for system-on-chip (SoC) designs. Other applications based on the sigma–delta modulation technique include digital telephony, digital signal processing, and instrumentation, digital audio and built-in self-test (BIST) for mixed-signal circuit. Testing ADCs is majorly limited to conventional static and dynamic testing. In this case, the signal generator needs to generate a stimulus with resolution at least four times higher than the ADC under test. In the case of dynamic testing, the test stimulus with known characteristic is applied to the ADC under test.

Testing such high-precision ADCs, however, requires high-performance and expensive test-platforms, which increases the test cost and eventually the final product cost comparing with all the kinds of analog to digital converters (ADCs), the architecture of the oversampled delta-sigma modulator will be the best choice.

One promising solution to this problem is BIST which utilizes on-chip resources (which could be either shared with functional blocks or dedicated BIST circuitry) to perform on-chip

stimulus generation and response acquisitions Under the BIST approach, the requirement on the external test equipment is less stringent. Furthermore, stimulus generation and response acquisition is more immune from environmental noise during the test process.

One of the challenges in the BIST approach for the mixed signal integrated circuit is - how to achieve high-precision on chip analog stimuli by smaller hardware cost as well as need to optimize output response analyzer for finding different parameter.

ORA (Output Response Analyzer) plays vital role to avoid depending on the BIST approach. It also reduces the test cost, and also increases the observability of the circuit under test which improves the fault coverage but accuracy and observability is not fully achieved yet. Special design need to require applied to overcome these problems.

Testing analog and mixed-signal (AMS) circuits is very costly and troublesome because of the requirements of high quality analog stimuli and ultra-low noise testing environment.

Furthermore, the numbers of testing parameters for AMS products are usually quite large, which considerably increase the test time. The too high test cost shrinks profit margins of high-end AMS products such as high-resolution Σ-Δ ADCs. Making testing Σ-Δ ADC cheaper and simpler without compromise of the testing accuracy thereby becomes an important issue for industry. Built-in-self-test (BIST) and design-for-digital-testability (DfDT) techniques can help to address high testing cost. The DfDT structures for Σ-Δ modulators are very appealing approaches. With a few additional analog switches, the DfDT structures can reconfigure the Σ-Δ modulator to accept Σ-Δ modulated bit-streams as the test stimuli in the test mode. The single-bit feature of the digital stimuli ensures the generated test stimuli are purely linear. The digital stimuli also have very high in-band signal-to-noise-and-distortion ratio (SNDR) owing to the noise shaping and oversampling nature of Σ-Δ modulation. Hence, expensive AMS automatic testing equipment (ATE) is no longer necessary. Since the DfDT structures reuse most of the circuit components of the ADC under test (AUT) in both the normal mode and the test mode, they provide many additional benefits such as high fault observability, high measurement accuracy, and the capability of conducting at-speed tests. To further reduce the test cost, making the DfDT Σ-Δ modulator built-in self-testable is preferable. This can be done by integrating the digital stimulus generator (DSG) and the digital output response analyzer (ORA) with the DfDT AUT. Such a BIST design needs no ATE at all. Hence, the only test cost is the added BIST circuitry. The digital resonator embedded with a digital Σ-Δ modulator well suits for implementing the required DSG for the DfDT Σ-Δ AUT. The hardware cost is low since the design eliminates the need for parallel multiplier. Besides, the amplitude and frequency of the generated Σ-Δ modulated bit stream are well controlled if the stimulus frequency is not too high. With respect to the ORA, a conventional approach is to analyze the output of the AUT in frequency domain using Fast Fourier Transform (FFT) analysis. However, performing FFT is too costly because conducting FFT requires lots of hardware resources such as bulky memory and a complex CPU/DSP. Alternatively, controlled sine wave fitting (CSWF) method that calculates the SNDR of the AUT in time domain can also be adopted. The CSWF method benefits from no output waveform have to be temporarily stored. As a result, the BIST circuitry can be made much smaller. Another method proposed a BIST Σ-Δ ADC prototype based on the CSWF method. The same DfDT second-order Σ-Δ modulator in is used as the modulator under test (MUT), and an FPGA board implements the decimation filter and the BIST circuitry. Experimental results of different technique show that the BIST design can accurately calculate the test parameters such as:-

- The offset
- The gain error
- The SNDR, and
- The dynamic range of the Σ-Δ AUT for the 1kHz tests.

Yet the hardware overhead can be further reduced.

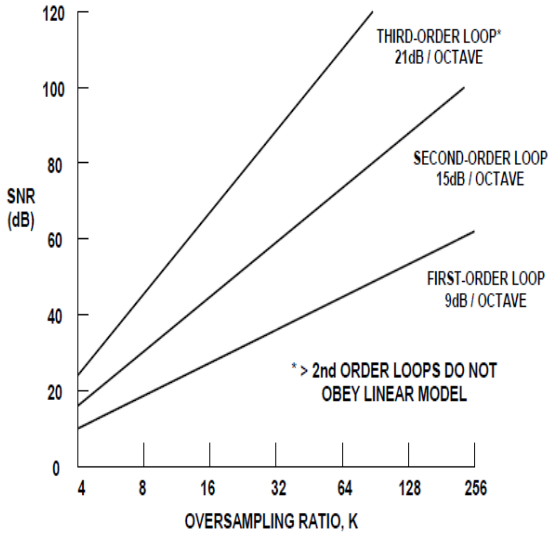

Fig1: SNR Vs Oversampling Ratio for First, Second, and Third-Order Loop

1.4 Built-in-Self-Test

- A built-in self-test (BIST) or built-in test (BIT) is a mechanism that permits a machine to test itself.
- Engineers design BISTs to meet all requirements such as:
  high reliability
  lower repair cycle times
- And Constraints such as:
  limited technician accessibility
  cost of testing during manufacture

BIST Architectures

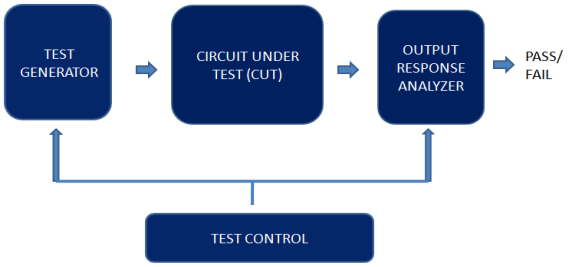

Fig2: Architecture of Built-in-Self-Test

2. A BRIEF REVIEW OF THE WORK ALREADY DONE IN THE FIELD

Status of recent research

We have studied research papers of various journals and conferences published on this research area. To have an idea of the status of recent research, below is the survey report of existing literatures.

Chaudhari et.al.(2013) proposed the design of a first order single bit Sigma-Delta ADC which is realized using CMOS technology. In this paper, first Order Sigma-Delta ADC is implemented in a standard 0.18um CMOS technology. The Design and Simulation of the first order Modulator is done using Mentor Graphics Tool. 1st order single bit Sigma Delta ADC Modulator is implemented using ±1.8 power supply and the simulation results are plotted using tools. This paper is first elaborate about ADC types and Classification among Nyquist rates and Oversampling ADCs. Further, a design of 1-bit Sigma Delta ADC is to be proposed which consists of Op-amp as a key component in Sigma delta ADC. Op-amp at integrator stage is having Gain Bandwidth (GB) of 5MHz, output resistance is 10KΩ, and power dissipation is 2.806 mW[1].

Kook et al.(2013), proposed a dynamic specification testing and diagnosis of high precision ΣΔ ADC. For the high resolution testing ADC require high end tester to ensure their performance according to the specification. The optimized stimulus generated in this paper was modeled as a 14-b signal with 80 dB SNR. To test the 300 DUTs regression based testing and model-parameter computation based testing was done.[2]

Ren et.al(2013) described the design of single loop two-order Delta-Sigma modulator with feed forward structure. Oversampled analog-to-digital converters based on second-order delta-sigma modulation are attractive for VLSI implementation because they are especially tolerant of circuit non-idealities and component mismatch. The noise shaping and oversampling are used in this modulator, the oversampling rate (OSR) is 256 and the resolution could reach 14 bits. The integrally design of Delta-Sigma modulator is argued in deep in the paper, since the behaviour model is tested efficiently using Simulink, the time of design has been cut to the bone. As the fully differential structure is used, the system inhibits the ability of common-mode interference improved and the sampling rate is also raised, the fully differential switching capacity structure is used in circuit design of modulator. And because of the fully differential structures, the input noise is reduced, the output slewrate of op-amp is greatly improved and the whole circuit is more stable. The 0.5 μm CMOS process is used in simulation of circuit, the results of simulation are shown that the amplifier gain is 82.3 dB, the Phase Margin is 71.34°, the output slewrate of op-amp is 202 V/μs, the unit GainBandWidth is 102 MHz. the whole circuit of modulator is tested with 10.24 MHz of the clock frequency, the SNDR reached to 93.2 dB, the Dynamic Range (DR) is 100 dB. In summary, this Delta-Sigma modulator could be used in Portable, Audio system etc[3].

Ting et al. (2011) discussed the structure of the output response analyzer (ORA) circuit for analog-to-digital converters (ADCs) built-in self-test (BIST) in which ADC static parameters, i.e., offset error, gain error, and nonlinearity errors, are directly obtained from the sine-wave histogram test. The appropriate approximations of the testing parameters reduce difficulties in designing the complete ORA circuit. In addition, the feature of reusable hardware in the calculation of sine-wave reference histograms and the computing capability of ADCs' parameters further improves the ORA design. The developed ORA circuits are synthesized in a 0.18-μm technology to analyze the outputs of an 8-bit ADC to verify the designs [4]

Trivedi et.al.(2011) presented a simulation and the designing overview of 2nd order sigma delta ADC. This shows the effectiveness of the simulation tool MATLAB. Through which we evaluate the SNR up to 97db. A digitally programmable Delta-Sigma modulator for 4G radios is presented in the paper. [5]

Eloued et al.(2009) ,designed a high level modelling of a ΣΔ modulator for the test of SNDR BIST. This is one of the technique in which analogue test signal is generated by using digital test pattern generator and converting the response into digital signature and is then compared with the expected ones. To test the efficiency, a high level description with VHDL-AMS for ΣΔ modulator was developed. This was done to obtain a fast and accurate modulator [6].

Hong et al.(2009) presents a prototype for BIST ΣΔ ADC. The BIST circuitry uses the proposed modified controlled sine wave fitting (CSWF) to calculate the signal power and total harmonic-distortion-and-noise power in the time domain. The BIST circuit is digital and the hardware overhead is as low as 11.9 K gates. The proposed BIST implementation gave a SNDR of 74.3 dB while the conventional FFT analysis resulted in a 74.6 dB SNDR of the same test. [7]

U.K. et.al.(2007) proposed a novel comparator architecture for high speed operation in low voltage environment. Comparison of different performances with a conventional regenerative comparator shows a speed-up of 41%.The proposed comparator is embedded in a continuous time Sigma-delta ADC so as to reduce the quantizer delay and hence minimizes the excess loop delay problem. An enhanced performance of 1dB in the dynamic range of the ADC is achieved with the proposed comparator. We have implemented this ADC in a standard single-poly 8-Metal 0.13μm UMC process. The complete system operates at 1.2V supply providing a dynamic range of 32dB consuming 720μW of power and occupies an area of 0.1mm2. [9].

Hong et.al (2006), gave a scheme of cost effective output response analyzer for ΣΔ modulation based BIST system. This paper gave an alternative approach of calculating SNDR by eliminating the use of FFT in frequency domain by proposing ORA using sine wave fitting procedure to calculate the signal power total-harmonic-distortion and noise power in time domain. When the amplitude of the input signal ranging from -60 to -4 dBFS is applied the result of ORA and FFT for SNDR has a maximum difference of 1.33 dB and a minimum difference of 0.02 dB in simulation as well as the mean and standard deviation results are 0.64dB and 0.36dB respectively.[11]

Jesus et.al (2005), presented a high-level synthesis of switched-capacitor, switched-current and continuous-time ΣΔ Modulator using SIMULINK-based time-domain behavioural model, in which the limiting factor using S-function blocks increases the computational efficiency. The combination of high accuracy, less CPU time and interoperability of different circuit together with the efficiency of the optimization engine makes the proposed tool an advantageous alternative for ΣΔ synthesis. Moreover, this is the first tool dealing with the synthesis of ΣΔ modulators using discrete and continuous time circuit technique.[12]

Toner et al.(1993), proposed a BIST scheme for an SNR test of a ΣΔ analog to digital converter, where direct and indirect cost estimation was done by the means of signal to noise ratio of an ADC. In this experiment, different alternatives for extracting the SNR of the ADC had been discussed. A prototype board was designed to allow 220 bits of the ADC which was supplied by the Bell-Northern Research(BNR), was a telecommunication ΣΔ converter which had been tested and verified to have an SNR of 78dB. However, in this experiment it was only able to achieve about 67dB.[13]

Noteworthy Contribution in the Field of Proposed Work

Lusi et al. (2006), designed a built-in-self test for signal to noise distortion ratio in ΣΔ ADC. The testing of analogue and mixed-signal circuit is done by second order ΣΔ modulator. The modulator samples the audio input signal at a clock frequency of 12288 KHz. A 4-stage decimation filter eliminates the out-of-band noise and frequency is reduced to provide a 16-bit output at a rate of 48 KHz, while the SNDR obtained by the simulations is 96.37 dB. If the memory is present on-chip then it can be reused to store the output test response as well as the sinusoidal reference signal. The calculation of SNDR and resolution had been done by using the BIST architecture with or without memory [10].

Hung et al.(2009) ,demonstrated a fully integrated BIST Σ−Δ ADC with a wide test bandwidth and high test accuracy. The proposed BIST procedure alleviates the possible overloading issues and reduces the number of setup parameters per test. The new BSG design with the proposed third-order Σ−Δ modulator extends the test bandwidth by a factor of 2. Experimental results shown here that SNDR differences between BIST results and the corresponding FFT results are less than 3 dB within a test bandwidth of 17 kHz, which is very close to the rated passband of the AUT. The hardware overhead of the proposed BIST design only consists of 13,300 gates, making it very suitable for embedded BIST applications. The BIST design can be applied to the Σ−Δ ADCs with other DfDT structures such as the decorrelating DfDT structure. [07]

Verma et.al (2014) designed a graphical user interface for second order Σ−Δ ADCs to check the non-idealities of the circuit. The model is based on the behavioural modelling of the parameters with the help of Matlab -Simulink and the parameters like Signal to Noise Ratio (SNR) & Effective Number of Bits (ENOB) (which in turn gives the Resolution) was calculated. The value of SNR and ENOB are found to be 107.88 dB and 17.61 bits respectively in comparison to the 89.4, 94.7 dB & 14.56, 15.44 bits respectively, which was found in the previous reference. Since the value of SNR and ENOB are increased it makes the signal power and Resolution better.[14]

3. PROBLEM IDENTIFICATION

1. On Chip area overhead is somewhat reduced while excluding memory element but accuracy of SNDR of sigma delta ADC is degraded.

2. It is hard to detect nonlinearity using two tone on more Multi-tone test signal for an Inter modulation test of sigma delta Modulator.

3. High level description with VHDL-AMS and modelling for ΣΔ modulator is not fully achieved for Higher or order sigma delta modulator.

4. Prototype is not fast to model accurately sigma delta ADC.

4. OBJECTIVE OF THE PROPOSED RESEARCH WORK

1. To develop high level modelling of sigma delta ADC for achieving improved performance of sigma delta BIST.

2. To develop cost effective in terms of on-chip area reduction insight ΣΔ ADC BIST.

3. To test the circuit in less time.

4. To make the testing easier.

5. PROPOSED METHODOLOGY DURING THE TENURE OF RESEARCH WORK

Delta-sigma (ΔΣ; or sigma-delta, ΣΔ) modulation is basically a method for encoding analog signals into digital signals or higher-resolution digital signals into lower-resolution digital signals. Response Analyzer consists of the following blocks:

Response analyzer: is a digital block that realizes the decision function. The aim is to analyze the L length window output modulator bit stream and its corresponding data stored in the reference memory in order to determine static errors & determine dynamic error.
In our work we have included:

- ✓ Reference signal memory
- ✓ Output signal memory
- ✓ Digital analysis, to improve the accuracy.

The whole BIST system consists of:
-the Σ-Δ ADC,
-two bit-stream generators (BSGs) as the DSG,
-the ORA,
-the phase compensator, and
-an optional serial I/O interface.

Since the phase shift for the Σ-Δ modulator is almost a constant because of its over-sampling nature, the transfer function of the phase compensator is as simple as z^{-2}. Two identical BSGs are used. The first one is the stimulus bit-stream generator (SBSG) for generating the digital stimuli for the AUT. The second one is the reference bit-stream generator (RBSG) for generating the aforementioned digital reference signals. The amplitudes of the generated stimulus tones can be controlled. In particular, *AS* can be used to represent the amplitude of the stimulus tone generated by the SBSG, and *AR* for that by the RBSG[08].

The ORA can be used to determine:
-the offset,
-the amplitude of stimulus-tone response,
-the SNDR
-the THD+N power.
But in our work we will concentrate on the values of SNDR.

Following implementation tools that can be used:

1) **Front End Tools**

   a) VHDL
   b) Verilog

2) **Back End Tools**
   a) Zeni

b) Tanner
c) H-Spice
d) MATLAB/SIMULINK

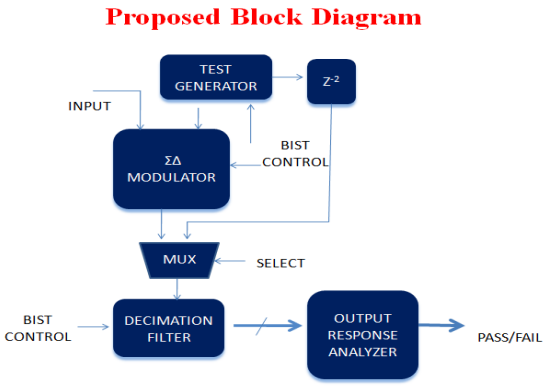

Fig : Proposed Block Diagram

6. EXPECTED OUTCOME OF THE PROPOSED WORK

After designing And Development of Output Response Analyzer for the BIST of ΣΔ Modulator, there would be some expected result:

- Resolution would be increased.
- Power consumption would be reduced.
- Testing time will be reduced.
- Signal to noise ratio would be increased.
- Expected performance would be compared with existing noteworthy contribution.

7. CONCLUSION

- Complexity will be reduced.
- Required area will be less.
- Power consumption will be less.
- Cost will be less.
- Testing time will be less.
- Area utilization will be high

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