Improved SNR and ENOB of Sigma-Delta Modulator for Post Simulation and High Level Modeling of Built-in-Self-Test Scheme

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ABSTRACT
This paper demonstrates a Graphical User Interface (GUI) of 2nd order Sigma-Delta modulator which is used to check the non-idealities of the circuit in BIST Scheme. High -level modeling of the parameters is done with the help of Matlab - Simulink and the parameters like Signal to Noise Ratio (SNR) & Effective Number of Bits (ENOB) are calculated. The value of SNR and ENOB are found to be 108 dB and 18 bits respectively Since the value of SNR and ENOB are increased it makes the respective signal power and Resolution better. The Graphical User Interface (GUI) of overall model has been successfully implemented after modeling of non-idealities for BIST technique not only avoids depending on the off-chip automatic test equipment (ATE) and reduces the test cost but increases the controllability and observability of the circuit under test also that improves the fault coverage .

Keywords
Sigma-Delta ADC; GUI; SNR; ENOB; BIST; DUT.

1. INTRODUCTION
Compared with Nyquist-rate ADCs, oversampling ADCs gets high resolution in spite of analog components it uses digital signal processing for performing analog-to-digital conversion and due to the oversampling delta-sigma ADCs, they do not need steep roll-off anti-alias filtering[4-5], which is the prime requirement of Nyquist-rate ADCs. Thus, higher order with better and higher linearity are hard to design and manufactured.

2. LOW-PASS SIGMA DELTA ADC
ADC based on 2nd order sigma-delta modulators is attractive for VLSI implementation because they are resistant to the circuit non- idealities and component mismatch. However, issues such as clock jitter and excess loop delay become great challenges to the designer [16], especially at high sampling frequency. Special design should be applied to overcome these problems. Sigma-delta modulation has demonstrated to be very suited interfaces for the implementation of various Analog to Digital in many electronic systems such as audio, biomedical . fig.1 below showing the different type of ADC in different frequency range.

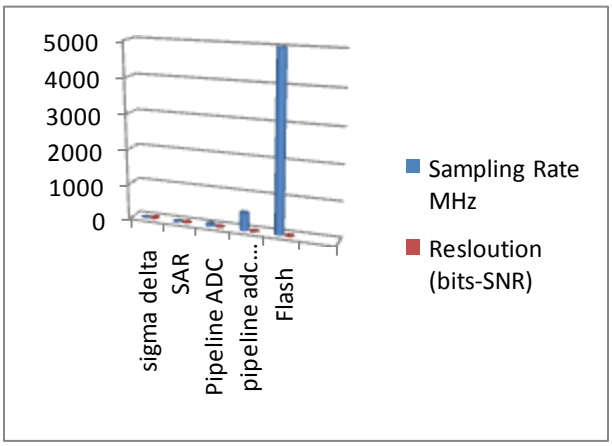

Fig 1: Applications of different types of ADC

Testing ADCs is mostly limited to conventional static and dynamic testing. Signal generator needs to generate a stimulus with resolution at least four times higher than that of the ADC under test in static test whereas in the case of dynamic testing, the test stimulus with known characteristics is applied to the ADC.

However, testing such high-precision ADCs requires high performance and expensive test-platforms, which further increases the test cost and final product as compared to all the kinds of ADCs[20]. One novel solution to this problem is built-in-self-test (BIST) which utilizes on-chip resources to perform on-chip stimulus generation and response acquisition under the BIST approach. With the advent of complementary-metal-oxide-semiconductor (CMOS) technology, BIST using digital signal; processing has become a viable solution for analog mixed-signal and SoC[22].

3. BIST (SIGMA-DELTA MODULATOR ANALOG-TO-DIGITAL CONVERTER)

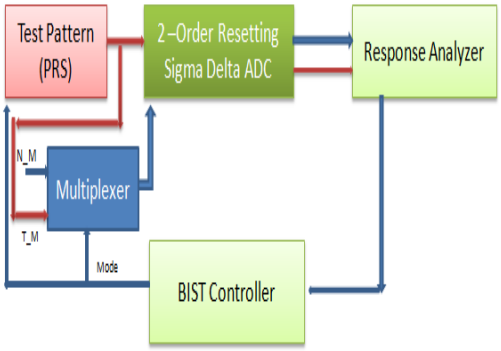

Fig 2. Built-in-Self-Test of Sigma-Delta Modulator Analog-to-Digital Converter

This work will use as BIST test for second order low pass DT sigma-delta modulator ADC and behavior modeling . The overall BIST structure for sigma-delta modulator includes following components[21-22]:

1. ***Test pattern Generation***: This component of the BIST structure converts digitized waveforms into analog signals. A semi -digital filter converts the digital values, memorized in the reference memory, to discrete analog levels. To generate the test stimulus signal, the stored digitized waveform is periodically applied to the modulator under test.
2. ***Mux* :** Multiplexer is switched between controlling function during the test mode and functional configuration during normal mode.
3. ***Design under Test (DUT)*:** DUT is basic testing block which is 2nd order Sigma –Delta DT modulator of ADC. We need to introduce the nonlinearity model parameter of ADC to obtain the dynamic error such as an effective number of bits (ENOB), total harmonic distortion (THD), SNR, etc.
4. ***BIST controller*:** The BIST controller is activated by the included boundary scan test access point (TAP) controller. Its activity is shown by a special output signal "test" and the functional pins enter an inactive state.
5. ***Response analyzer:*** This is used in evaluating the response of DUT analyzer to analyze the *L*-length window output modulator bit stream and its corresponding data stored in the reference memory in order to determine static and dynamic error.

4. FLOW DIAGRAM

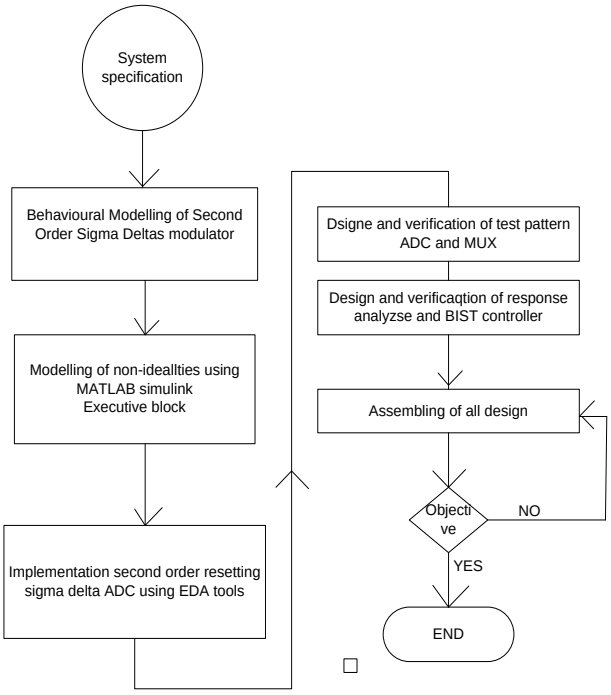

Fig.3 BIST Flow

5. DESIGN UNDER TEST (DUT)

Delta-sigma (ΔΣ; or sigma-delta, ΣΔ) modulation is used as DUT and method of encoding analog signals into digital signals or higher-resolution digital signals into lower-resolution digital signals.

A 2nd Order Sigma-Delta A/D Converter consists of the following

- A loop filter or loop transfer function H(s)
- A clocked quantizer feedback digital to analog converter (DAC).

The schematic of a first-order SC ΣΔ modulator is shown[11-12]. The main non-idealities appearing in the SC circuitry, which should be considered for accurate modelling, are as follows[13]:

1. Clock jitter
2. Switch thermal noise
3. Operational amplifier noise
4. Op-amp DC gain
5. Op-amp Bandwidth(BW)
6. ***Op-amp slew rate(SR)***

A loop filter H(s) provides a noise-shaping function for the analog input signal before it is sampled and quantized by an ADC. The digital output signal is then converted back to an analog signal by a DAC and feedback to the input for subtraction to form a closed-loop operation. The input signal is sampled after being filtered through the loop filter, significant suppression at aliasing frequencies can be obtained[14].

Proposed work will use 2nd order sigma -delta modulator ADC and system modeling of no idealities and simulation of modulator will be done. There are two integrators inside the

topology to realize the 2nd order system. Also the output noise value is less in less frequency.[2]

6. RESULTS

Table: Comparison of result

S. No.	Parameters	Previous Work[4]	Previous Work[5]	Our Work
1)	Bandwidth(BW in HZ)	22000	20000	20000
2)	Oversampling Ratio(R)	256	256	256
3)	No. of Samples (N)	2^14	2^14	2^14
4)	Slew Rate	17(V/us)	202(V/us)	250(V/us)
5)	GBW	100 MHz	102 MHz	150MHz
6)	SNR (in dB)	86.7	94.7	108
7)	ENOB(bits)	14.11	15.44	18

The basic GUI performs the following function

1) **For giving the inputs**: Here in this diagram it is clearly shown that 3 inputs namely Bandwidth, Oversampling Ratio(R) & No. of Samples (N) is inputted.
2) **For generating the Simulink Model**: After applying the inputs the Open Simulink Model Tab will open the Simulink model as shown below.
3) **For getting the output :** After the Simulink model runs we will get the output in the GUI.

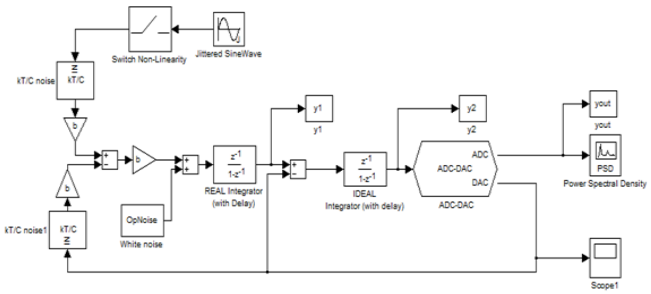

Fig .4: Simulink Model

4) **Outputs**

The basic design of the Simulink model along with the non - idealities is shown.

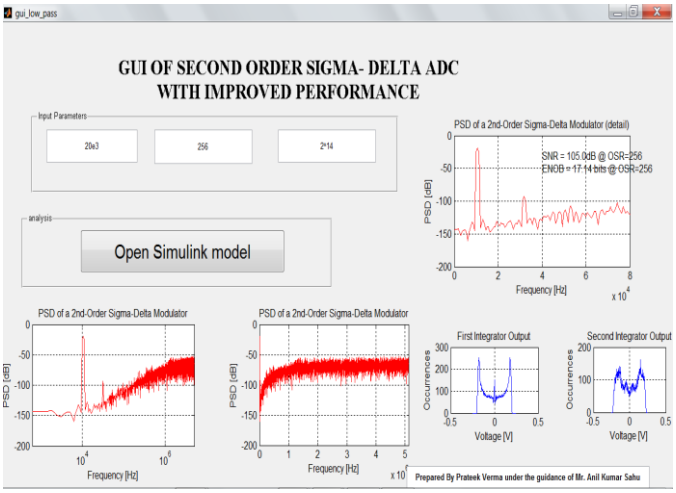

Fig. 5: GUI showing the output waveforms

```
** Simulation Parameters **
    Fs(Hz)=10240000
    Ts(s)=9.765625e-008
    Fin(Hz)=10625.0000
    BW(Hz)=20000
    OSR=256
    Gain(dB)=82
    Phase Margin(in Degrees)=71.340
    CMRR =93.400
    SNR(dB)=104.971
    Simulation time =0.690 min
```

Fig 6: Output of the command window of MATLAB

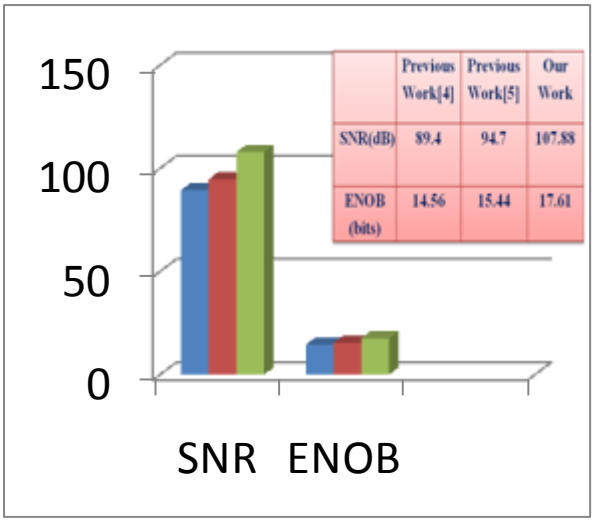

FIG.7 . BAR GRAPH SHOWING THE COMPARISON VALUE OF SNR & ENOB

7. CONCLUSIONS

With the help of 2nd Order low pass Sigma Delta analog to digital converter, we can improve the resolution and signal to noise ratio as well as we can reduce the power consumption and increase the ENOB. We have to take care of the Non-Idealities like clock jitter, excess loop delay etc so that it will not affect the performance of the circuit. Behavioral model of 2nd order low-pass sigma-delta modulator including the non-idealities (sampling jitter, thermal noise, op-amp noise, slew rate and bandwidth) are studied. Special design is being

applied to overcome the non-idealities. A GUI is has been made to calculate the SNR and ENOB of sigma- delta ADC.

Here the model is based on the behavioral modeling of the parameters with the help of Matlab- Simulink and the parameters like Signal to Noise Ratio (SNR) & Effective Number of Bits (ENOB) (which in turn gives the Resolution) are calculated. The value of SNR and ENOB are found to be 108 dB and 18 bits respectively in comparison to the 89.4, 94.7 dB & 14.56, 15.44 bits respectively of the previous work[16]. Since the value of SNR and ENOB are highest and it makes the respective signal power and Resolution better. In our work post -simulation of modulators will be done using the BIST approach, The method will be more effective in terms of area overhead and power consumption.

8. REFERENCES

[1] Verma, Prateek, and Anil kumar Sahu. "A Graphical User Interface(GUI) implemented Low-pass continuous time Sigma-delta ADC with improved SNR & ENOB." International Journal of Advanced Research in Computer Science and Software Engineering 4.6 (2014): 144-149.

[2] S. Yan, E. Sanchez-Sinencio "A continuous-time sigma-delta modulator with 88-dB dynamic range and 1.1-MHz signal bandwidth" IEEE Journal of Solid-State Circuits.Feb 2004.

[3] http://www.eeweb.com/blog/carmen_parisi/balancing-the-tradeoffs-in new-generation- adcs.

[4] Brigati, S., Francesconi, F., Malcovati, P., Tonietto, D., Baschirotto,A., & Maloberti, F. (1999, July). Modeling sigma-delta modulator non-idealities in SIMULINK (R). In Circuits and Systems, 1999. ISCAS'99.

[5] Bandopadyay, T. K., Manish Saxena, and Raghav Shrivastava. "Sigma Delta Modulator with Improved Performance through Evolutionary Algorithm." International Journal of Science and Research (IJSR) Volume 2 Issue 3, March 2013.

[6] Benabes, Philippe. "Accurate time-domain simulation of continuous-time sigma–delta modulators." Circuits and Systems I: Regular Papers, IEEE Transactions on 56.10 (2009): 2248-2258.

[7] Bolatkale, Muhammed. "A 4 GHz continuous-time ADC with 70 dB DR and 74 dBFS THD in 125 MHz BW." Solid-State Circuits, IEEE Journal of 46.12 (2011): 2857-2868.

[8] [Chaudhari, Jaydip H. "Design and Simulation of 1-bit Sigma Delta ADC in 0.18 um CMOS Technology." IJCAIT 2.1 (2013): 50-53.

[9] C. H. E. N. Zhicai, Mathew Bond, and Nijad Anabtawi. "Design of a Second Order Continuous Time Sigma Delta Modulator with Improved Dynamic Range." Final Project of Oversampling Class, Fall 2007 Arizona State University.

[10] Garcia, Julian, Saul Rodriguez, and Ana Rusu. "A Low-Power CT Incremental 3rd Order/spl Sigma//spl Delta/ADC for Biosensor Applications." Circuits and Systems I: Regular Papers, IEEE Transactions on 60.1 (2013): 25-36.

[11] Gerfers, Friedel, Maurits Ortmanns, and Yiannos Manoli. "A 1.5-V 12-bit power-efficient continuous-time third-order ΣΔ modulator." Solid-State Circuits, IEEE Journal of 38.8 (2003): 1343-1352.

[12] Hart, Adam, and Sorin P. Voinigescu. "A 1 GHz Bandwidth Low-Pass ADC With 20–50 GHz Adjustable Sampling Rate." Solid-State Circuits, IEEE Journal of 44.5 (2009): 1401-1414.

[13] Kumar, Y. B. N., et al. "A 1.96-mW, 2.6-MHz bandwidth discrete time quadrature band-pass ΣΔ modulator." Circuits and Systems (ISCAS), 2013 IEEE International Symposium on. IEEE, 2013.

[14] Lim, Huey Jen, Simon Sheung Yan Ng, and Minkyu Je. "Bandpass Continuous-Time Delta-Sigma Modulator for Wireless Receiver IC." International Journal of Information and Electronics Engineering, Vol. 3, No. 1, January 2013.

[15] Shaoyu MA, Yan Han, You Cai A 3.3V 18 Bit Digital Audio Sigma- Delta ADC in 0.18 um CMOS Process 2007.

[16] Prateek Verma, Anil Kumar Sahu, Dr. Vivek Kumar Chandra & Dr. G.R. Sinha "A Graphical User Interface Implementation of Second Order Sigma- Delta Analog to Digital Converter with Improved Performance Parameters"International Journal for Research in Applied Science & Engineering Technology (IJRASET) Volume 2, Issue 7, July 2014,ISSN: 2321-9653.

[17] Prateek Verma & Anil Kumar Sahu, A 22 kHz Bandwidth and 107dB SNR Low-pass Sigma-delta ADC. International Conference "SHAASTRATH" on 23rd - 24th March 2014 at Rungta Group of Institutions, Raipur

[18] Prateek Verma, Arun Kumar Sonwani & Anil Kumar Sahu, A 16 Bit ENOB and 98 dB SNR 2nd order Low-pass Sigma-delta ADC,International Conference on Emerging Trends in Electrical, Electronics, Instrumentation & Computer Engineering (ETEICE), BIT Raipur 27th March 2014

[19] SIMULINK and MATLAB Users Guides, The MathWorks, Inc.

[20] Drago Strle and Janez Trontelj, "High Level Simulation of Real Time BIST of Sigma Delta A/D Converters," International Conference on Synthesis ,Modelling ,Analysis And Simulation Method And application To Circuit Design , pp. 285-289, 2012.

[21] Jingbo Duan, Le jin, and Degan Chen, "INL based Dynamic Performace Estimation For ADC BIST ," IEEE conference on Circuit and System, pp. 3028-3031, 2010.

[22] Hsin Wen Ting, "An o/p Response Analyzer Circuit For ADC Built -in Self -Test," J, Electron test, vol. 27, pp. 455-464, 2011.

[23] Julian Garica and Ana Rusu, "Built in self Calibration For Process Variation In Single -Loop Continous Time Sigma Delta Modulators," ICESCS,IEEE, pp. 1136-1139, 2010.