Energy Saving using Data Encoding Scheme in Network-on-Chip for LDPC Application

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ABSTRACT
Communication subsystems such as routers and wired or wireless network interfaces consume more power in network on chip. With the target of reduction in power consumption in network on chip, three encoding schemes are presented in this paper. These schemes work at flit level which results in reduction of self and coupling transition without making modification in the link architecture and routers. Globally to defend memories from soft error correction codes have been used which make changes in logical value of memory cubicles without destructing the circuit. As memory expands, demand of complex decoder rises due to complex codes. One of such decoder is LDPC. We can apply these encoding schemes to linear density parity check (LDPC) codes. Power dissipation is reduced. The dynamic power value reduction is verified by using x-power analyzer tool.

Keywords
Network on Chip, LDPC Decoder, Switching and coupling activity, Encoding scheme.

1. INTRODUCTION
Network on chip also referred as communication subsystem, dissipate more power because of self-switching activity and coupling switching activity. According to Figure1 which represents NoC architecture, shaded circle refers to wireless hub and remaining hubs are wired. Consider 2nd hub is a destination and 7th hub is a source, if flit is transferred from source to destination, it will follow a particular path and switch from one router to another. Because of the switching activity, more delay is incurred which consumes more power in network on chip. If the raw computation horsepower seems to be unlimited, thanks to the ability of instancing more and more cores in a single silicon die, scalability issues, due to the need of making efficient and reliable communication between the increasing number of cores, become the real problem [1]. The network on- chip (NoC) design paradigm [3] is recognized as the most viable way to tackle with scalability and variability issues that characterize the ultradeep submicronmeter era. Nowadays, the on-chip communication issues are as relevant as, and in some cases more relevant than, the computation related issues [3] In fact, the communication subsystem increasingly impacts the traditionaldesign objectives, including cost (i.e., silicon area), performance, power dissipation, energy consumption,

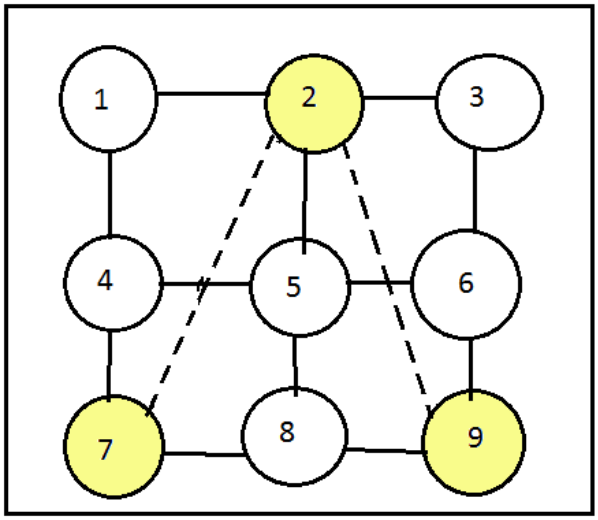

Figure1. NoC architecture

Reliability, etc. As technology shrinks, an ever more significant fraction of the total power budget of a complex many-core system-on-chip (SoC) is due to the communication subsystem. In this paper, we focus on techniques aimed at reducing the power dissipated by the network links. In fact, the power dissipated by the network links is as relevant as that dissipated by routers and network interfaces (NIs) and their contribution is expected to increase as technology scales [4]. In particular, we present a set of data encoding schemes operating at flit level and on an end-to-end basis, which allows us to minimize both the switching activity and the coupling switching activity on links of the routing paths traversed by the packets. The proposed encoding schemes, which are transparent with respect to the router implementation, are presented and discussed at both the algorithmic level and the architectural level, and assessed by means of simulation on synthetic and real traffic scenarios. The analysis takes into account several aspects and metrics of the design, including silicon area, power dissipation, and energy consumption. The results show that by using the proposed encoding schemes the dynamic power value reduction is verified by using x-power analyzer tool.. We briefly discuss related works in Section II, while Section III presents an overview of the proposed data encoding schemes. The proposed data encoding schemes are described in Section IV. In Section V, the results for the hardware overhead, power and energy savings, and performance reduction of the proposed data encoding schemes are compared with those of other approaches. Finally, this paper is concluded in Section VI.

2. RELATED WORKS AND CONTRIBUTIONS

This category of encoding is not suitable to be applied in the deep submicronmeter technology nodes where the coupling capacitance constitutes a major part of the total interconnect capacitance. This causes the power consumption due to the coupling switching activity to become a large fraction of the total link power consumption, making the aforementioned techniques, which ignore such contributions, inefficient. The works in the second category concentrate on reducing power dissipation through the reduction of the coupling switching. The switching activity is reduced using many extra control lines. The data are both odd inverted and even inverted, and then transmission is performed using the kind of inversion which reduces more the switching activity. The coupling switching activity is reduced in this paper, we use a simpler decoder while achieving a higher activity reduction. Let us now discuss in more detail the works with which we compare our proposed schemes. The number of transitions from 0 to 1 for two consecutive flits (the flit that just traversed and the one which is about to traverse the link) is counted. If the number is larger than half of the link width, the inversion will be performed to reduce the number of 0 to 1 transitions when the flit is transferred via the link. This technique is only concerned about the self-switching without worrying the coupling switching. Note that the coupling capacitance in the state-of–the-art silicon technology is considerably larger (e.g., four times) compared with the self-capacitance, and hence, should be considered in any scheme proposed for the link power reduction.

In addition, the scheme was based on the hop-by-hop technique, and therefore, encoding/decoding is performed in each node. The scheme presented in dealt with reducing the coupling switching. In this method, a complex encoder counts the number of Type I (Table I) transitions with a weighting coefficient of one and the number of Type II transitions with the weighting coefficient of two. If the number is larger than half of the link width, the inversion will be performed. In addition to the complex encoder, the technique only works on the patterns whose full inversion leads to the link power reduction while not considering the patterns whose full inversions may lead to higher link power consumption. Therefore, the link power reduction achieved through this technique is not as large as it could be. This scheme was also based on the hop-by-hop technique. Technique only works on the patterns whose full inversion leads to the link power reduction while not considering the patterns whose full inversions may lead to higher link power consumption. Therefore, the link power reduction achieved through this technique is not as large as it could be. This scheme was also based on the hop-by-hop technique. In another coding technique presented, bunches of four bits are encoded with five bits. The encoded bits were isolated using shielding wires such that the occurrence of the patterns “101” and “010” were prevented. This way, no simultaneous Type II transitions in two adjacent pair bits are induced. This technique effectively reduces the coupling switching activity. Although the technique reduces the power consumption considerably,

Table1. Possibilities of transition

Time	Normal			Odd Inversion		
	Type I			Type II, III, IV		
t - 1	10, 01	01, 10, 00, 11	11, 00	11, 00	00, 11, 01, 10	10, 01
t	10, 01	01, 10, 00, 11	11, 00	11, 00	00, 11, 01, 10	10, 01
	TI*	TI**	TI***	Type III	Type IV	Type II
	Type II			Type I		
t - 1	01, 10			01, 10		
t	10, 01			11, 00		
	Type III			Type I		
t - 1	00, 11			00, 11		
t	11, 00			10, 01		
	Type IV			Type I		
t - 1	00, 11, 01, 10			00, 11, 01, 10		
t	00, 11, 01, 10			01, 10, 00, 11		

It increases the data transfer time, and, hence, the link energy consumption. This is due to the fact that for each four bits, six bits are transmitted which increases the communication traffic. This technique was also based on the hop-by-hop approach. A coding technique that reduces the coupling switching activity by taking the advantage of end-to-end encoding for wormhole switching has been presented in [23]. It is based on lowering the coupling switching activity by eliminating only Type II transitions. In this paper, we present three encoding schemes. In Scheme I, we focus on reducing Type I transitions while in Scheme II, both Types I and II transitions are taken into account for deciding between half and full invert, depending the amount of switching reduction. Finally, in Scheme III, we consider the fact that Type I transitions show different behaviours in the case of odd and even inverts and make the inversion which leads to the higher power saving.

3. OVERVIEW OF THE PROPOSAL

The basic idea of the proposed approach is encoding the flits before they are injected into the network with the goal of minimizing the self-switching activity and the coupling switching activity in the links traversed by the flits. In fact, self-switching activity and coupling switching activity are responsible for link power dissipation. In this paper, we refer to the end-to-end scheme. This end-to-end encoding technique takes advantage of the pipeline nature of the wormhole switching technique. Note that since the same sequence of flits passes through all the links of the routing path, the encoding decision taken at the NI may provide the same power saving for all the links. For the proposed scheme, an encoder and a decoder block are added to the NI. Except for the header flit, the encoder encodes the outgoing flits of the packet such that the power dissipated by the inter-router point-to-point link is minimized.

4. PROPOSED ENCODING SCHEMES

In this section, we present the proposed encoding scheme whose goal is to reduce power dissipation by minimizing the coupling transition activities on the links of the interconnection network. Let us first describe the power

model that contains different components of power dissipation of a link. The dynamic power dissipated by the interconnects and drivers is

$$P = [T0\rightarrow1\ (Cs + Cl) + TcCc]\ V2ddFck \qquad (1)$$

where $T0\rightarrow1$ is the number of $0 \rightarrow 1$ transitions in the bus in two consecutive transmissions, Tc is the number of correlated switching between physically adjacent lines, Cs is the line to substrate capacitance, Cl is the load capacitance, Cc is the coupling capacitance, Vdd is the supply voltage, and Fck is the clock frequency. One can classify four types of coupling transitions. A Type I transition occurs when one of the lines switches when the other remains unchanged. In a Type II transition, one line switches from low to high while the other makes transition from high to low. A Type III transition corresponds to the case where both lines switch simultaneously. Finally, in a Type IV transition both lines do not change. The effective switched capacitance varies from type to type, and hence, the coupling transition activity, Tc, is a weighted sum of different types of coupling transition contributions. Therefore

$$Tc = K1T1 + K2T2 + K3T3 + K4T4 \qquad (2)$$

Where Ti is the average number of Type i transition and Ki is its corresponding weight. According to [26], we use $K1 = 1$, $K2 = 2$, and $K3 = K4 = 0$. The occurrence probability of Types I and II for a random set of data is 1/2 and 1/8, respectively. This leads to a higher value for $K1T$ 1 compared with $K2T$ 2 suggesting that minimizing the number of Type I transition may lead to a considerable power reduction. Using (2), one may express (1) as

$$P = [T0\rightarrow1\ (Cs + Cl\ ) + (T1 + 2T2)\ Cc]\ V\ 2ddFck. \qquad (3)$$

According to [3], Cl can be neglected

$$P \propto T0\rightarrow1Cs + (T1 + 2T2)Cc. \qquad (4)$$

Here, we calculate the occurrence probability for different types of transitions. Consider that flit $(t - 1)$ and flit (t) refer to the previous flit which was transferred via the link and the flit which is about to pass through the link, respectively. We consider only two adjacent bits of the physical channel. Sixteen different combinations of these four bits could occur (Table I). Note that the first bit is the value of the generic ith line of the link, whereas the second bit represents the value of its $(i + 1)$th line. The number of transitions for Types I, II, III, and IV are 8, 2, 2, and 4, respectively. For a random set of data, each of these sixteen transitions has the same probability. Therefore, the occurrence probability for Types I, II, III, and IV are 1/2, 1/8, 1/8, and 1/4, respectively. In the rest of this section, we present three data encoding schemes designed for reducing the dynamic power dissipation of the network links along with a possible hardware implementation of the decoder.

A. Scheme 1

In scheme 1, our main goal is to reducing the number of Type 1 transitions and Type 2 transitions. Type 1 transitions is converted into Type III and Type IV transitions and Type II transitions is converted into Type I transitions. This scheme compares the two data‘s based on to reducing the link power reduction by doing odd inversion or no inversion operation.

$$T_y > T_x \qquad (5)$$

$$T_y > 0.5\ (w\text{-}1) \qquad (6)$$

The general block diagram in Fig.2. is same for scheme 1, scheme 2 and scheme 3. The w-1 bit is given to the one input of the binary to gray conversion block.

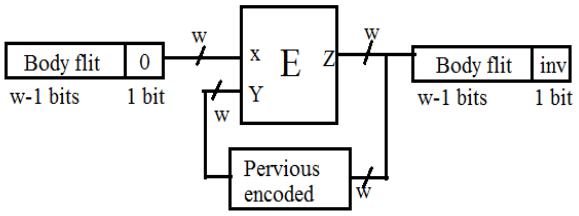

Figure2. Encoder Block Diagram

This block converts the original binary input into gray output. The output of the gray code is given as input of encoder block and another input of the encoder block is the previously encoded output. The encoder block compares these two inputs and performing the any one of the inversion based on the transition types. The block E is vary for all the three schemes. Comparing the current data and previous encoded data to decide which inversion is performed for link power reduction. Here the TY block this takes two adjacent bits from the given inputs. From these two input bits the TY block checks what type of transitions occurs, whether more number of type 1 and type 2 transitions is occurring means it set the output state to 1, otherwise it set the output to 0. The odd inversion is performed for these type of transitions. Then the next block is the Majority code it checks the state, if the number of one‘s is greater than zeros or not and it implemented using a simple circuit. The last stage using the XOR circuits, these circuit is used to perform the inversion on odd bits. The decoding is performed by simply inverts the encoder circuit when the inverting bit is high.

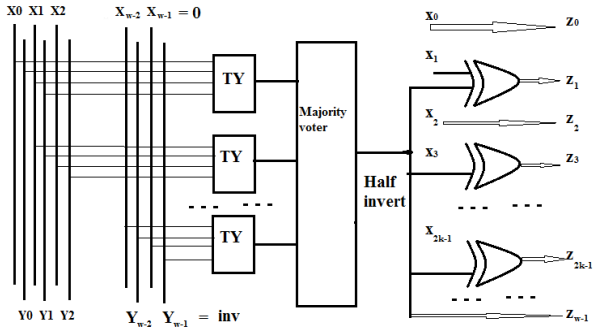

Figure3. Encoder architecture scheme I

B. Scheme 2

In scheme II, our main goal is to reducing the number of Type II transitions. Type II transitions are converted into Type IV transitions. This scheme compares the two data‘s based on to reducing the link power reduction by doing full inversion or odd inversion or no inversion operation.

$$T_2 > T_{4**} \qquad (7)$$

Full and odd inversion based this advanced encoding architecture consist of w-1 link width and one bit for inversion

bit which indicate if the bit travel through the link is inverted or not. W bits link width is considered when there is no encoding is applied for the input bits. Here the TY block from scheme 1 is added in scheme 2. This takes two adjacent bits scheme 1 is added in scheme 2. This takes two adjacent bits

from the given inputs. From these two input bits the TY block checks what type of transitions occurs. We have T2 and T4 * blocks which determines if any of the transition types T2 and

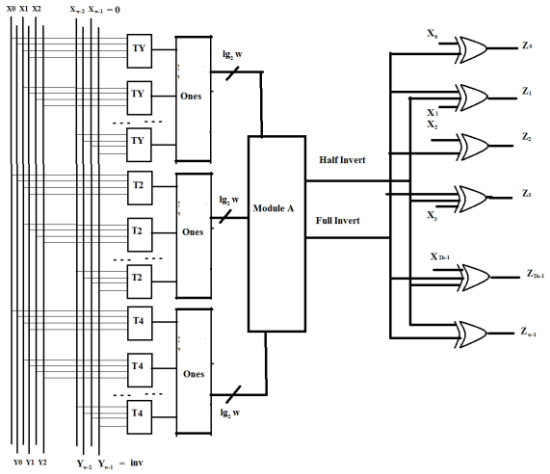

Figure4. Encoder architecture scheme 2

T4 *occur based on the link power reduction. The number of ones blocks in the next stage. The output of the TY, T2 and T4 * send through the number of one‘s blocks. The output of the ones block is log 2 w. The first ones block is used to determine the number of transitions based on odd inversion. The second ones block determines the number of transitions based on the full inversion and the then another one ones block is used to determine the number of transitions based on the full inversion. These inversions are performed based on the link power reduction. Based on these ones block the Module A takes the decision of which inversion should be performed for the link power reduction. For this module is satisfied means the output is set to _1‘. None of the output is set to _1‘ if there is no inversion is takes place. The module A is implemented using full adder and the block diagram of the decoder is shown in Fig.5. The w-1 bits input is applied in the decoder circuit and another input of the decoder is previous decoded output. . The decoder block compares the two input data‘s and inversion operation is performed and w-1 bits output is produced. The remaining one bit is used to indicate the inversion is performed or not. Then the decoder output is given to the gray to binary block. This block converts the gray code into original binary input. In decoder circuit diagram (Fig.6.) consist of TY block and Majority vector and

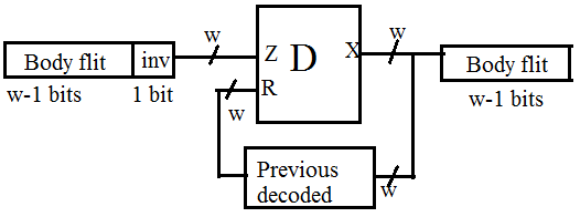

Figure5. Decoder Block Diagram

Xor circuits. Based on the encoder action the TY block is determined the transitions. Based on the transitions types the majority blocks checks the validity of the inequality given by (2). The output of the majority voter is given to the Xor circuit. Half inversion, full inversion and no inversion is performed based on the logic gates.

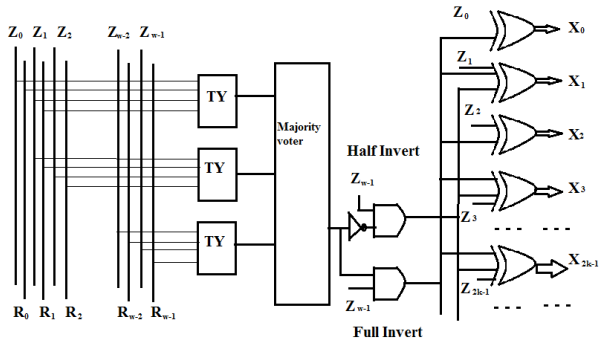

Figure6. Internal View of the Decoder Block

C. . Scheme 3

In scheme III, we are adding the even inversion into scheme II. Because the odd inversion converts Type I transitions into Type II transitions. From table II, T1 */T1 *** are converted into Type IV/Type III transitions by the flits is even inverted. The link power reduction in even inversion is larger than the Odd inversion.

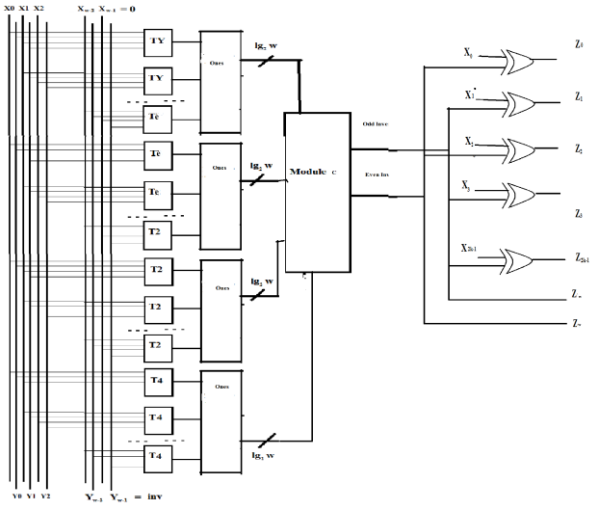

Figure7. Encoder architecture for scheme 3

The encoding architecture (Fig.7) in scheme III is same of encoder architecture in scheme I and II. Here we adding the Te block to the scheme II. This is based on even invert condition, Full invert condition and Odd invert condition. It consist of w-1 link width input and the w bit is used for the inversion bit. The full, half and even Inversion is performed means the inversion bit is set _1‘, otherwise it set as _0‘.The TY, Te and T4** block determines the transition types T2, Te and T4**. The transition types are send to the number of ones block. The Te block is determined if any of the detected transition of types T2, T1** and T1**. The ones block determines the number of ones in the corresponding transmissions of TY, T2, Te and T4**. These number of ones is given to the Module C block. This block check if odd, even, full or no invert action corresponding to the outputs _10‘, _01‘, _11‘or _00‘respectively, should be performed. The decoder architecture of scheme II and scheme III are same.

Table 2. Even Inversion

Time	Normal			Even Inversion		
	Type I			Type II, III, IV		
t - 1 t	01, 10 00, 11	00, 11, 01, 10 10, 01, 11, 00	00, 11 11, 00	01, 10 10, 01	00, 11, 01, 10 00, 11, 01, 10	00, 11 11, 00
	TI*	TI**	TI***	Type II	Type IV	Type III
t - 1 t	Type II 01, 10 10, 01			Type I 01, 10 00, 11		
t - 1 t	Type III 00, 11 11, 00			Type I 00, 11 01, 10		
t - 1 t	Type IV 00, 11, 01, 10 00, 11, 01, 10			Type I 00, 11, 01, 10 10, 01, 11, 00		

5. RESULT

Result of Scheme1

Waveform shows final odd inverted output (out) of internal input signals, clk, rst ,enb which is necessary for circuit simulation. Figure 8. Represent result of scheme I.

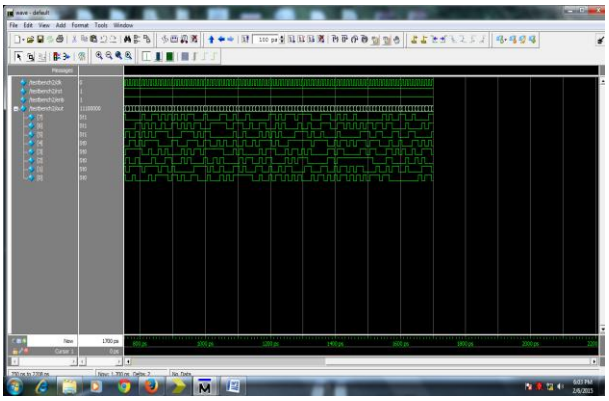

Figure8. Result of Scheme I

Extension Results(LDPC) Decoder

Normal Decoder with schemeI

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	74	4656	1%
Number of 4 input LUTs	131	9312	1%
Number of bonded IOBs	91	232	39%
Number of GCLKs	1	24	4%

LDPC Deoderc with schemeI

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	37	4656	0%
Number of Slice Flip Flops	44	9312	0%
Number of 4 input LUTs	55	9312	0%
Number of bonded IOBs	20	232	8%
Number of GCLKs	1	24	4%

6. CONCLUSION

We are presenting 3 encoding schemes which highly aims at reduction in power dissipation in network on chip. This paper also helps in understanding how to lessen the usage of dynamic power by lessening the use of transition on network on chip. This paper concludes about the proposed LDPC Decoder which is designed using Verilog HDL and simulated using modelsim Software and Synthesized by Xilinx 9.1iin which the result shows that the proposed decoder requires fewer OR, IOBs and latency compared with existing methods or previous normal Encoder.

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